

TRIGGERS FOR HADRON COLLIDER PHYSICS

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UNIVERSITY OF FLORIDA (GO GATORS!)

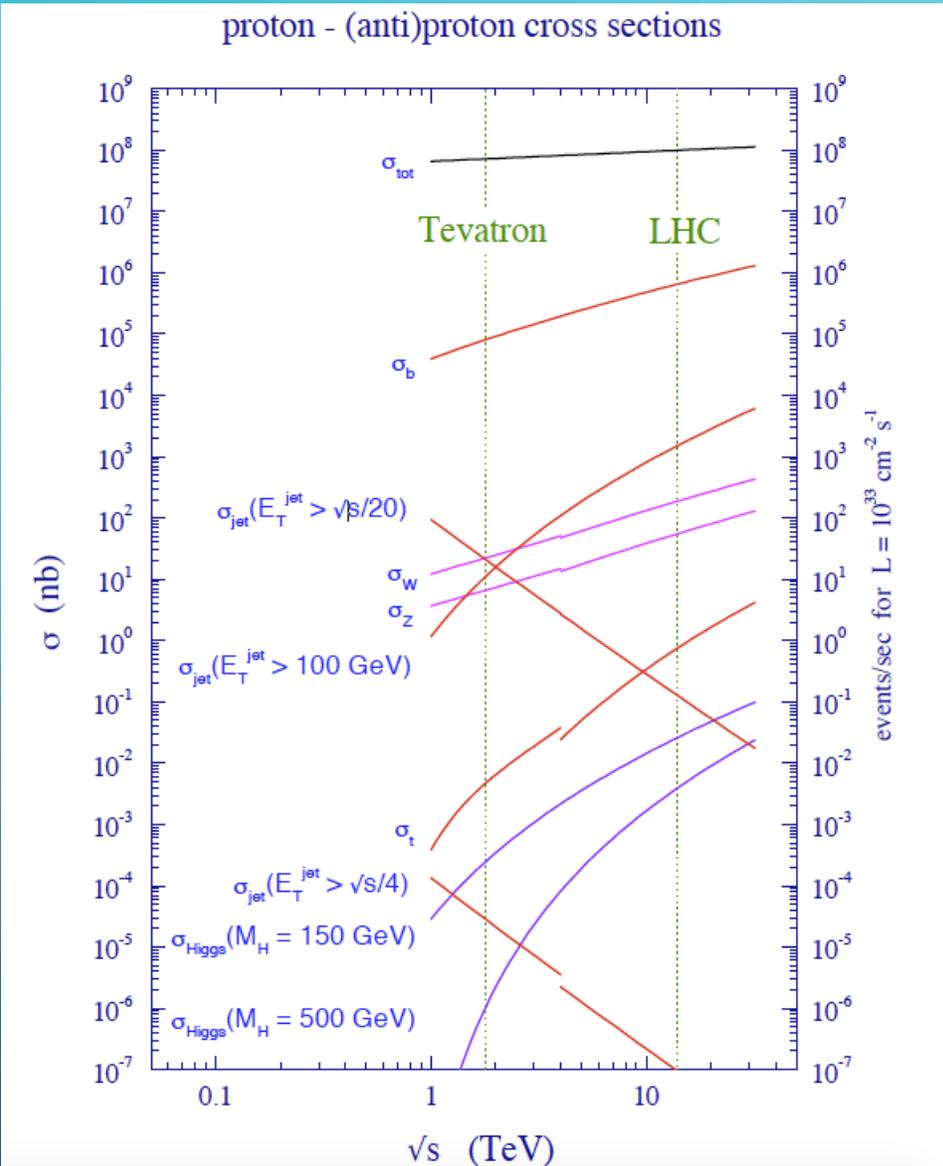


HADRON COLLIDER CROSS SECTIONS & RATES



for $L = 2 \times 10^{34} \text{ Hz/cm}^2$

arXiv: 1002.0274v2



← Total collision rate: 2 GHz

← b quark rate: 10 MHz

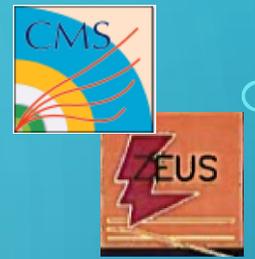
← W boson rate: 4 kHz

← Higgs boson rate: 1 Hz

Keep for storage

Challenge of triggering at hadron colliders: cannot keep all physics processes in order to collect enough data on interesting rare processes

TRIGGER SYSTEMS AT COLLIDER EXPERIMENTS



- Segmented into multiple levels, with decreasing output rates and longer processing times (latencies)
- Level-1:
 - **Custom electronic designs** for maximum throughput and shortest latencies (microseconds).
 - Initially custom chips (**ASICs**) to meet needs, but later commercial programmable logic (**FPGAs**) became available
 - Processing logic done in a **maximally parallel way** for shortest latency
- Level-2:
 - Combination of custom electronics and commercial computing equipment
- Level-3:
 - **Commercial computing clusters** of up to thousands of CPUs and about a second per event processing time

COST EFFECTIVE WITH MULTIPLE STAGES



The image shows a SpaceX Falcon Heavy rocket launch of GPS III SV01. The rocket is ascending vertically, leaving a large plume of white smoke and a bright orange flame trail. The launch is taking place at night or dusk, with the ocean and a dark landscape visible in the background. The rocket's reflection is visible in a body of water in the foreground.

TELEMETRY DATA:

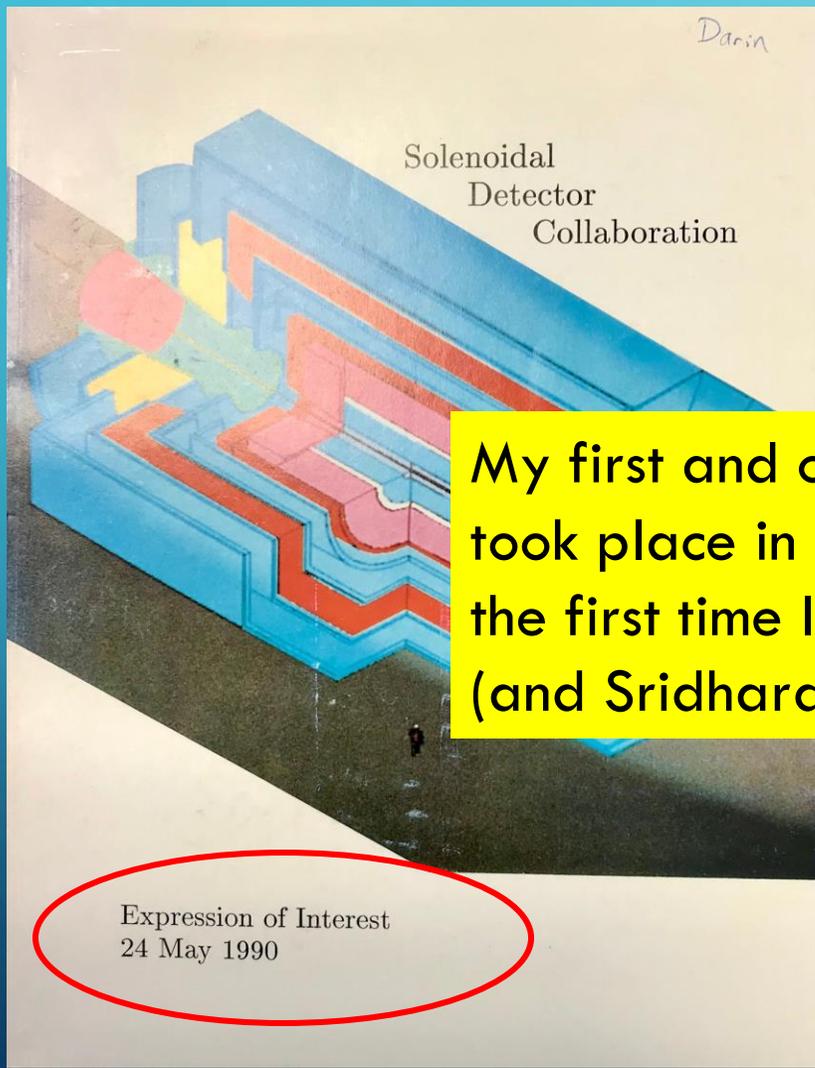
| STAGE 2 | TELEMETRY |
|------------|-----------|
| SPEED | ALTITUDE |
| 00131 km/h | 00.2 km |

MISSION TIMELINE:

- LAUNCH: GPS III SV01
- LIFTOFF
- MAIN ENGINE CUTOFF
- SECOND STAGE ENGINE STARTUP
- SECOND STAGE ENGINE CUTOFF
- DEPLOY

SPACEX

BUT BEFORE THERE WAS CMS & LHC, THERE WAS SDC & THE SSC PLAN...



My first and only SDC meeting took place in 1993, and was the first time I met Wesley (and Sridhara)

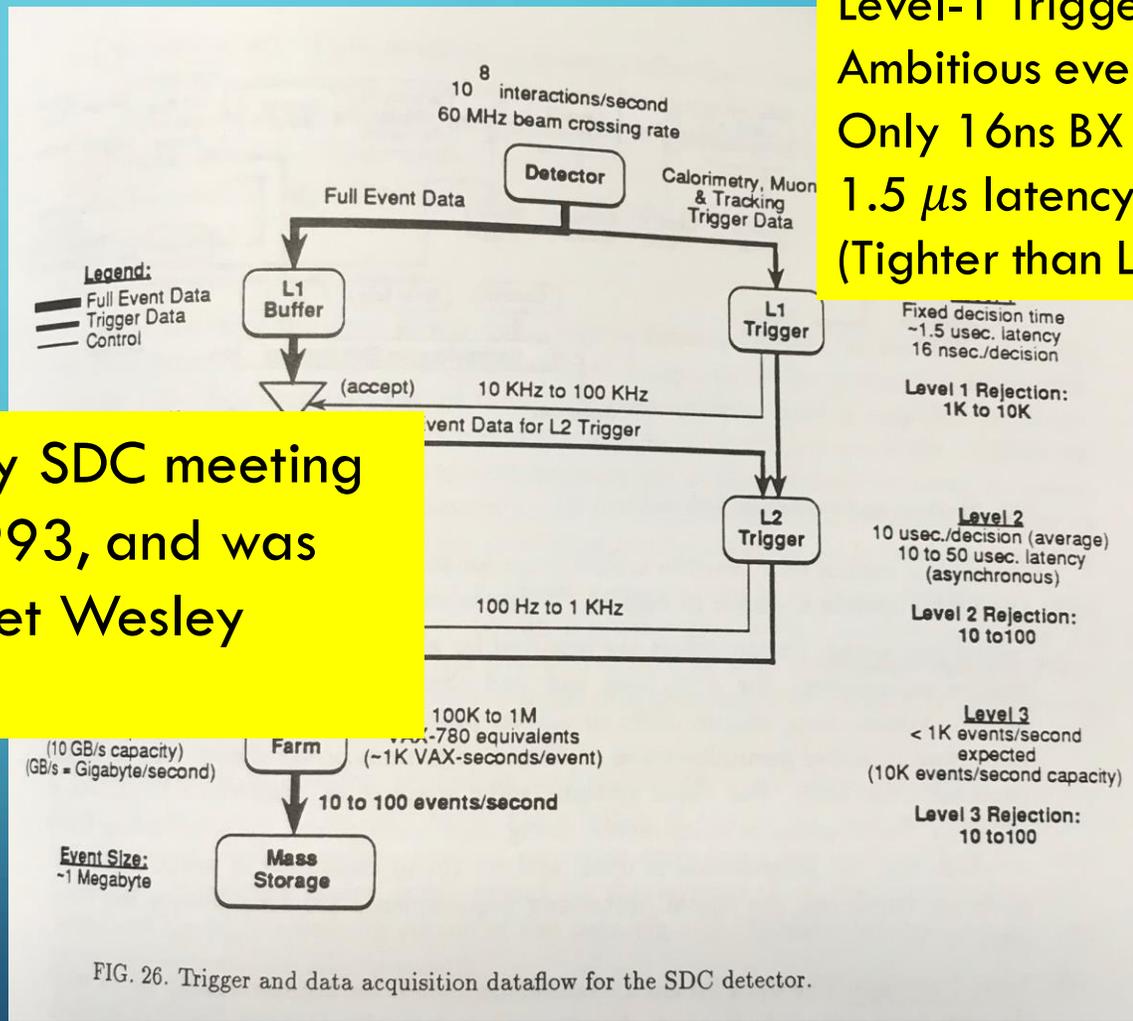
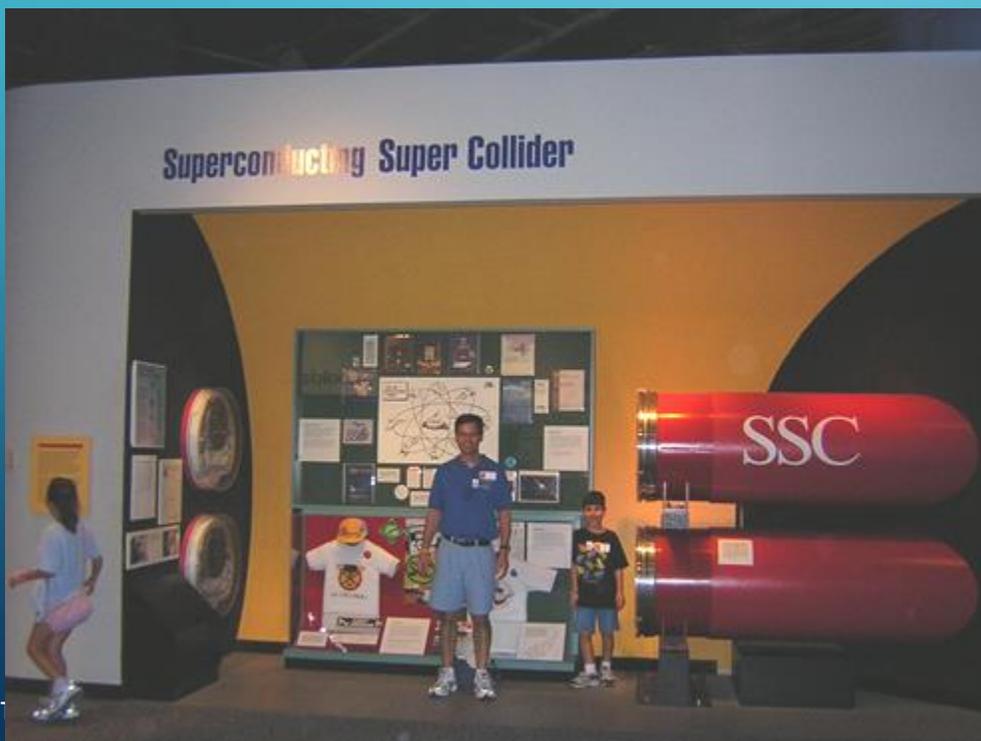


FIG. 26. Trigger and data acquisition dataflow for the SDC detector.

NOW A FOOTNOTE IN THE SMITHSONIAN



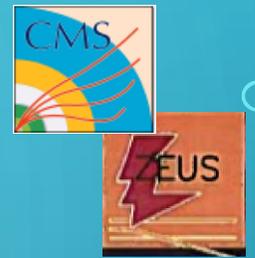
- The Superconducting Super Collider
 - 40 TeV center-of-mass energy
 - Waxahachie, TX
 - R.I.P. 1993



Circa 2005

DARIN ACOS

HERA ELECTRON-PROTON COLLIDER



@ DESY,
Hamburg
Germany

Launched 1992

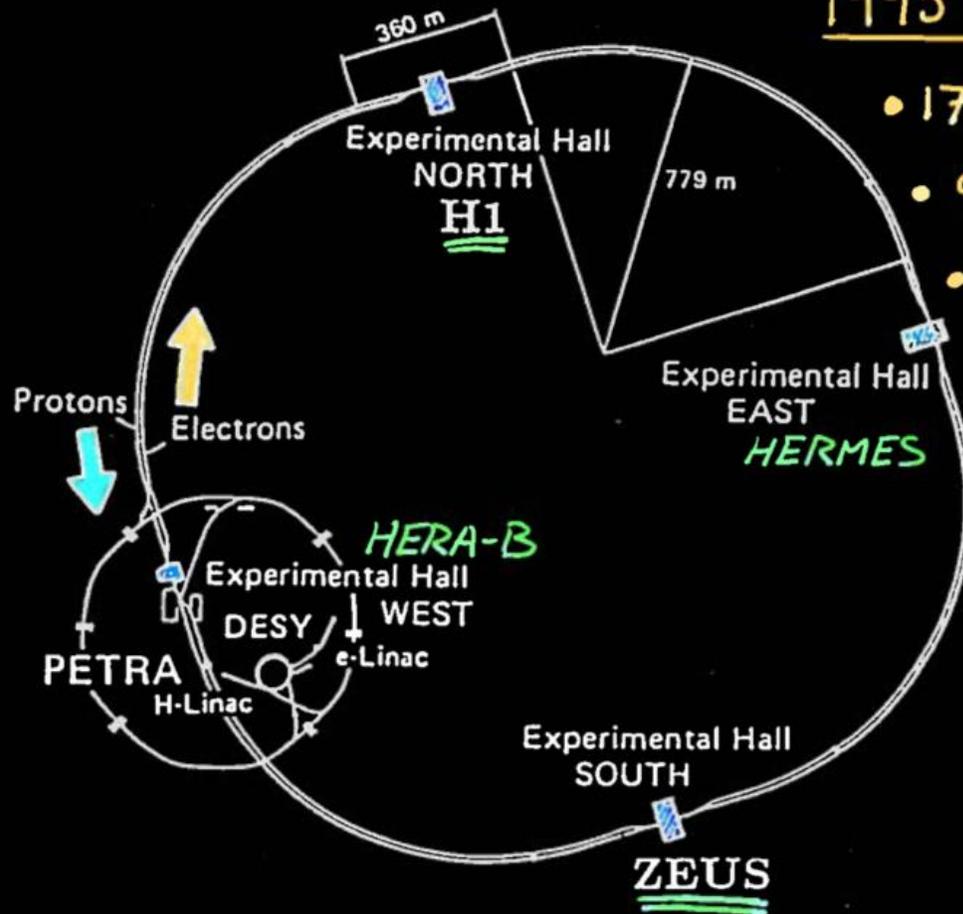
$E_e = 27.5 \text{ GeV}$
 $E_p = 820\text{-}920 \text{ GeV}$

HERA

1995 Parameters:

- 174 bunches
- 96ns spacing
- $I_e = 30 \text{ mA}$
- $I_p = 65 \text{ mA}$

Still tight bunch spacing! Significantly less than Tevatron Run 1 (microseconds)

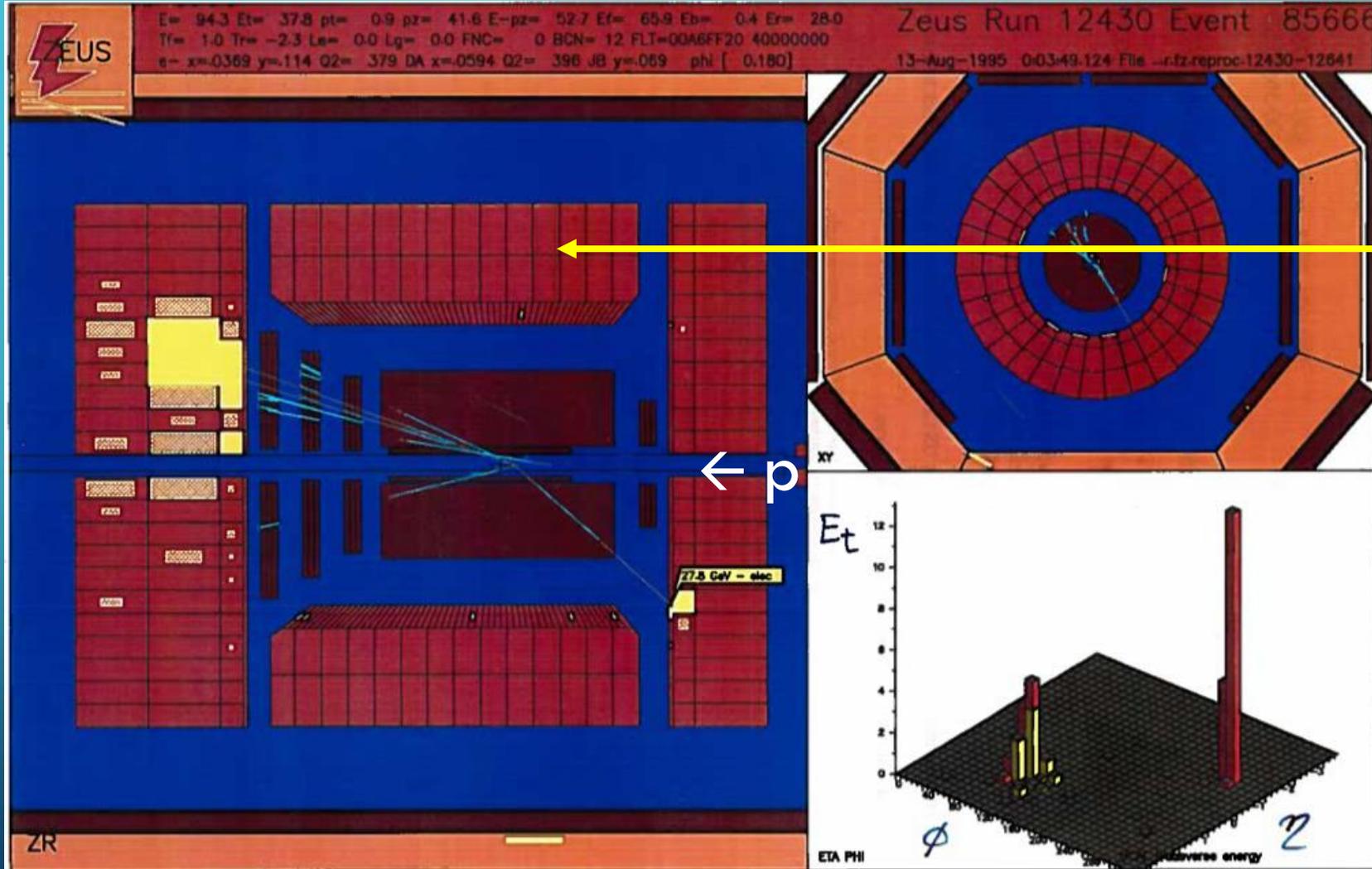


Trigger system development benefited from Supercollider efforts

ZEUS DEEP INELASTIC SCATTERING EVENT



LAZE event display



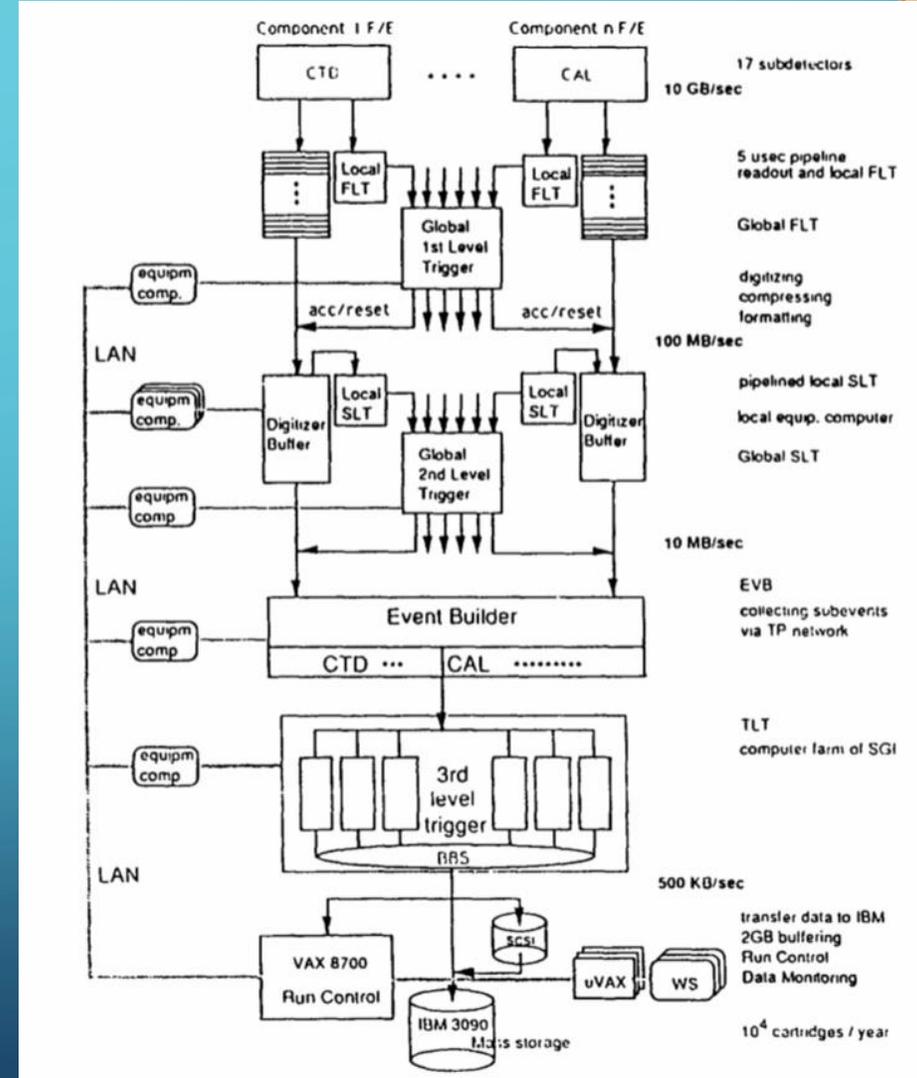
Uranium-Scintillator calorimeter. Barrel built by US groups ("AMZEUS")

Data processed by calorimeter trigger

ZEUS TRIGGER SYSTEM



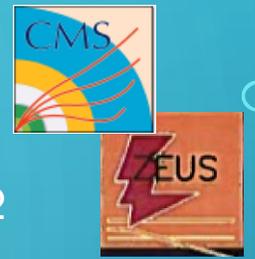
- Three Level Trigger system
- Dominant background at HERA is beam gas interactions which occur at a typical rate of few hundred kHz
 - Only half of a hadron collider...
- Level-1 takes in data at **10 MHz** beam crossing input rate, and reduces to < 1 kHz
 - Total Latency $5.5 \mu\text{s}$
 - Calculations are **pipelined** in 96 ns steps (i.e. no dead time)
- “Transputers” comprise Level-2, 3 and Event Builder
 - Early parallelized real-time computing platform



NIM A332 (1993) 253

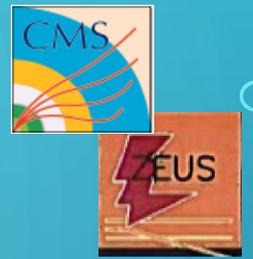
THE ZEUS CALORIMETER FIRST LEVEL TRIGGER (CFLT)

NIM A360 (1995) 322

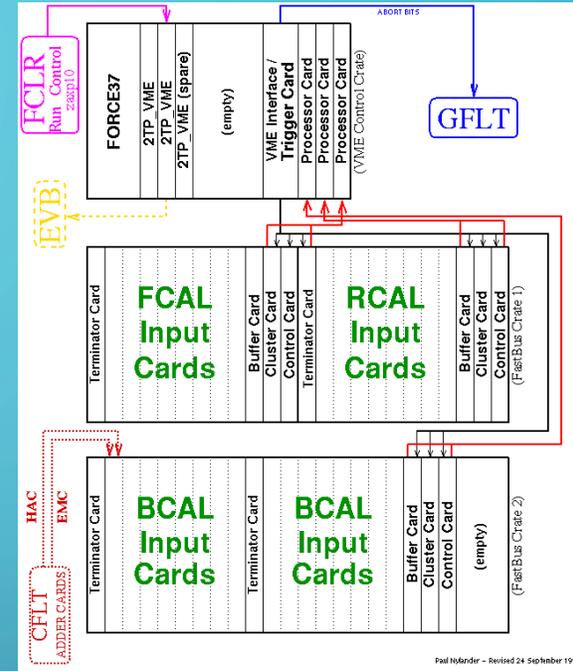


- A Wisconsin, Argonne effort
- Processes 896 trigger towers (from calo PMT signals) in 16 regions (and VME crates) of 7x8 towers
 - Each crate has 14 Trigger Encoder cards (digitizes calo data) and 2 Trigger Adder cards to perform sums
- Determines the total, transverse, and missing transverse energy, and identifies isolated electrons and muons(!), and sums energies in programmable subregions.
 - The Calorimeter Trigger essentially IS the Level-1 trigger, since no dedicated muon trigger
 - Thankfully a MIP trigger is enough, as background rates at HERA are low

THE ZEUS FAST CLEAR, A “LEVEL-1.5”

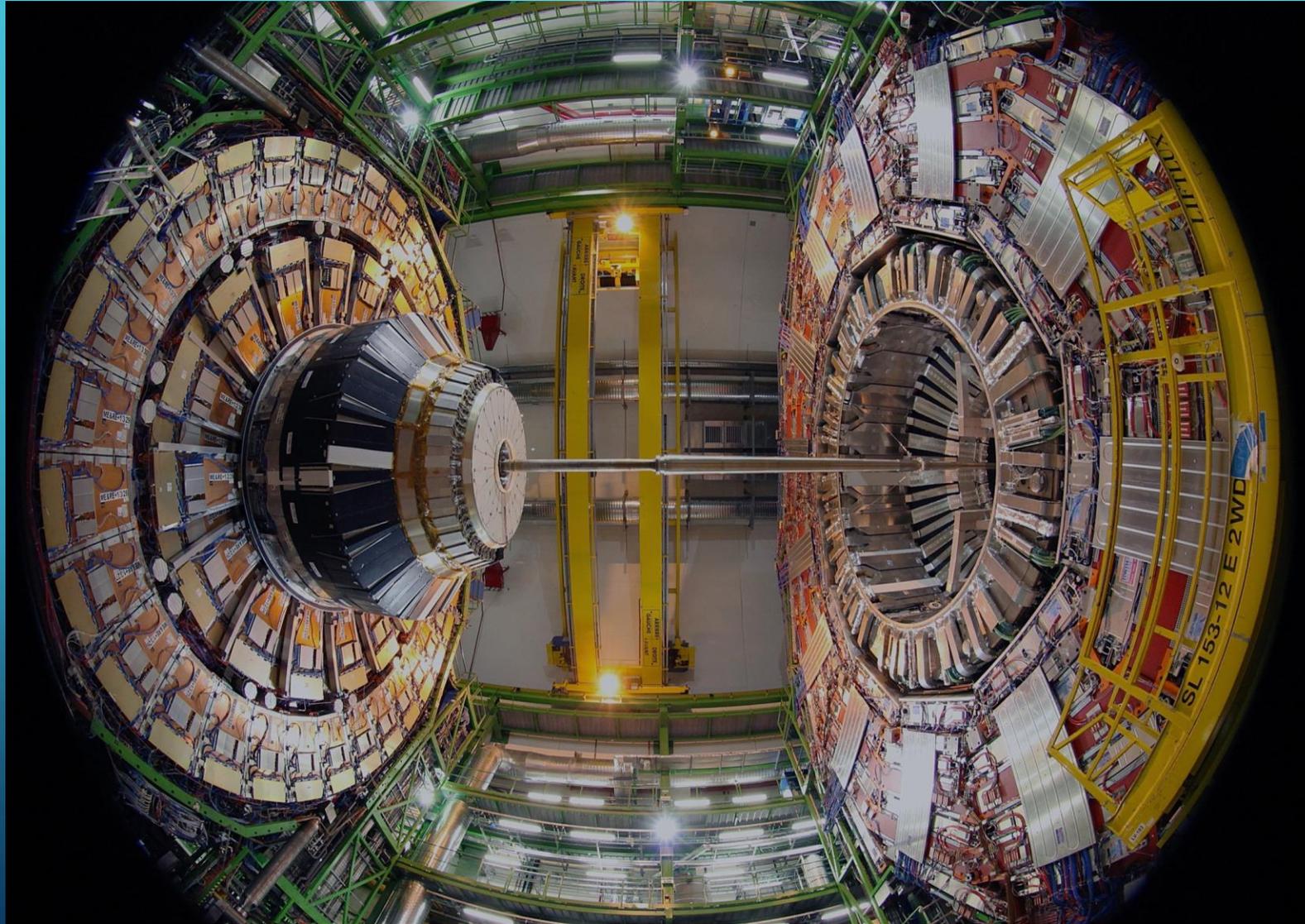


- Developed by OSU
- Cluster finder for **electrons** and **jets**
- The Fast Clear processed the calorimeter trigger data from the Wisconsin electronics during the time the DAQ data were being digitized.
 - Larger $15 \mu\text{s}$ latency for processing
 - The Fast Clear would abort the detector digitization to reduce the rate of data going to the second level global trigger.
- In addition to clustering, Fast Clear calculated $E-P_z$ from the calorimeter data, and used it to reduce the rate of Neutral Current triggers



Paul Nylander - Revised 24 September 1997

THE CMS EXPERIMENT

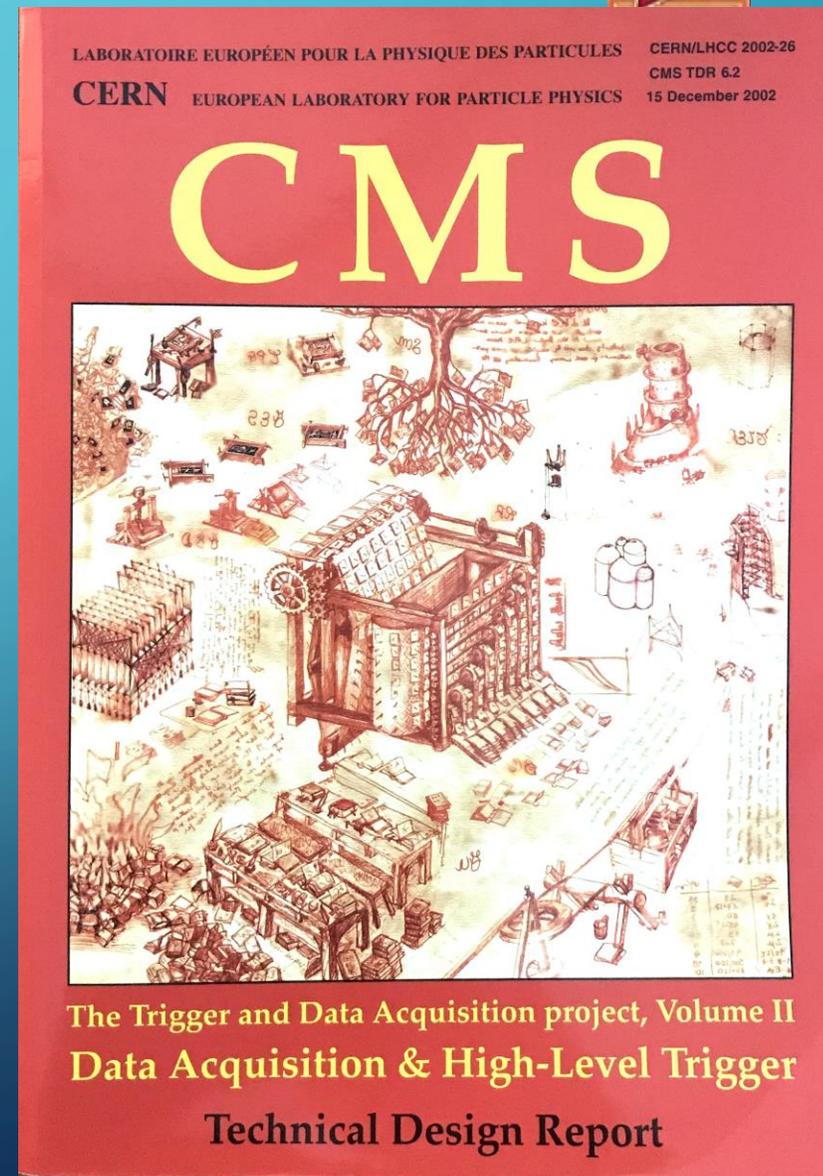
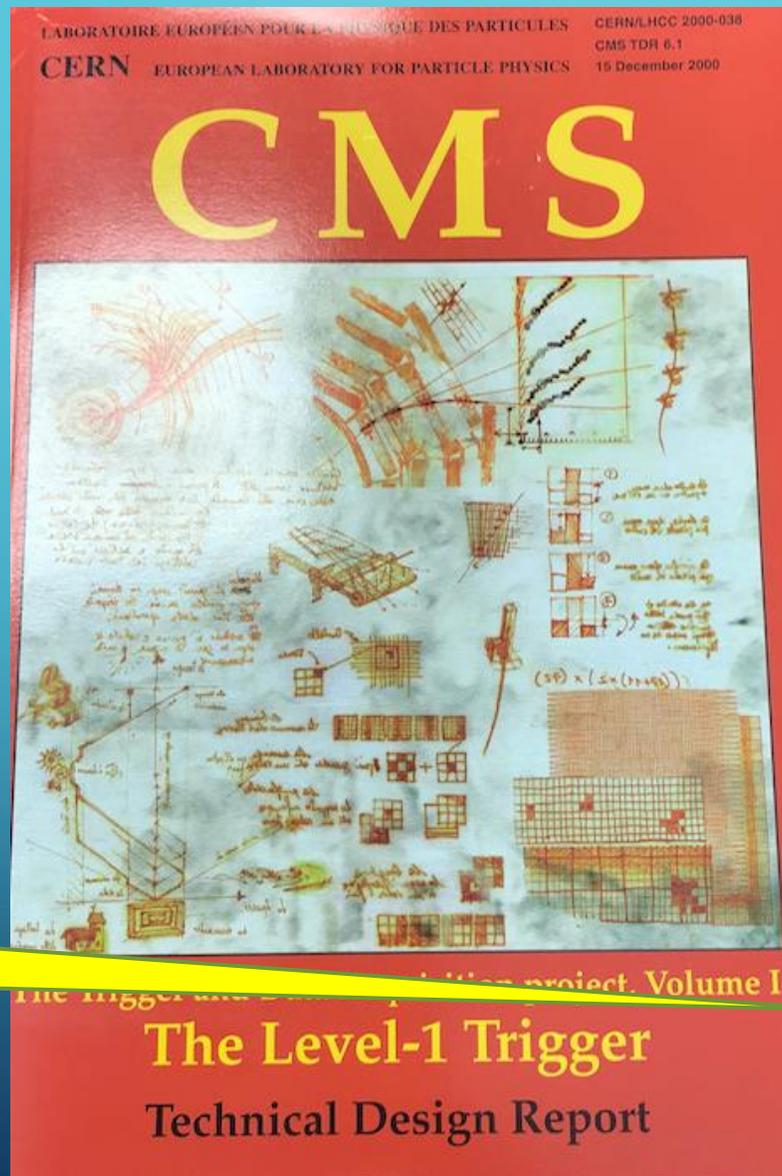


FIRST CMS LEVEL-1 TRIGGER, TDR 2000



Simulation results obtained using the first C++ framework of CMS: "ORCA".

Revised in 2002 in DAQ/HLT TDR

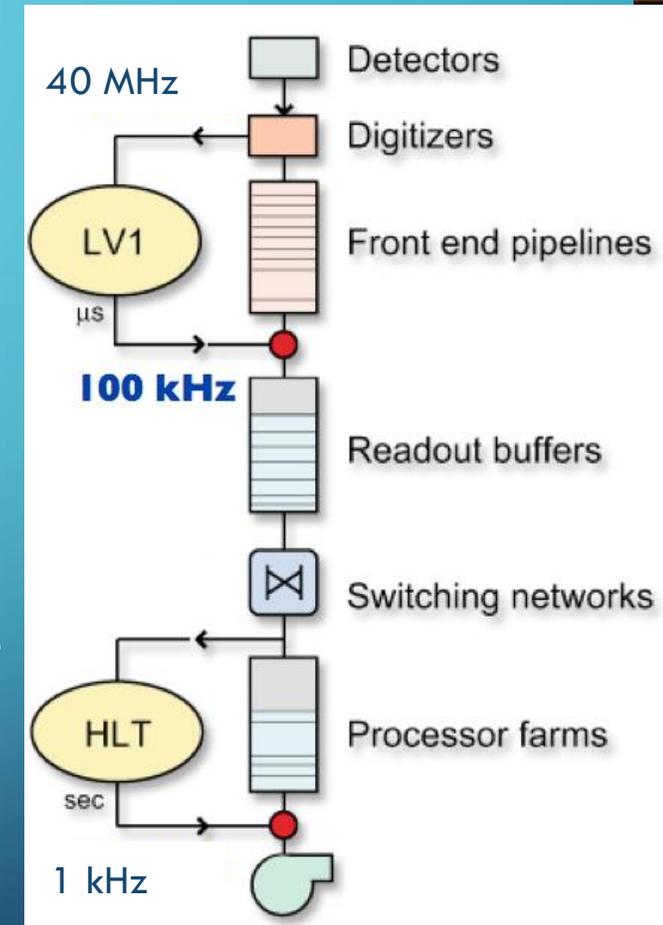


CMS TRIGGER ARCHITECTURE



- Only two levels*:
 - **Level-1**: custom electronics to reduce the data from a collision rate of **40 MHz to no more than 100 kHz** for the detector readout electronics, with only a $4 \mu\text{s}$ latency (buffer depth)
 - **High Level Trigger (HLT)**: event filter farm comprised of commercial CPUs running software to further reduce event rate to storage to an average of **$\sim 1 \text{ kHz}$** (for LHC Run 2)

*CMS was a leader in adopting a powerful HLT.



COLLIDER TRIGGER COMPARISONS

One to two orders of magnitude increase

| | Tevatron / CDF (2004) | LHC / CMS (2018) |
|--|------------------------------|-------------------------|
| Beam Energy | 1 TeV | 6.5 TeV |
| Inst. Lumi. (cm⁻²s⁻¹) | 10 ³² | 200X 2x10 ³⁴ |
| Bunch xing freq / Time spacing | 2.5 MHz / 400 ns | 16X 40 MHz / 25 ns |
| L1 pipelined ? | No (Run 1) | Yes |
| L1 output rate | 25 kHz | 4X 100 kHz |
| L2 output / HLT input | 400 Hz | 250X 100 kHz |
| L3 output rate | 90 Hz | 10X 1000 Hz |
| Event size | 0.2 MB | 5X 1 MB |
| Filter Farm | 250 CPUs | 40X O(10 000) CPUs |

FIRST CMS L1 TRIGGER ARCHITECTURE

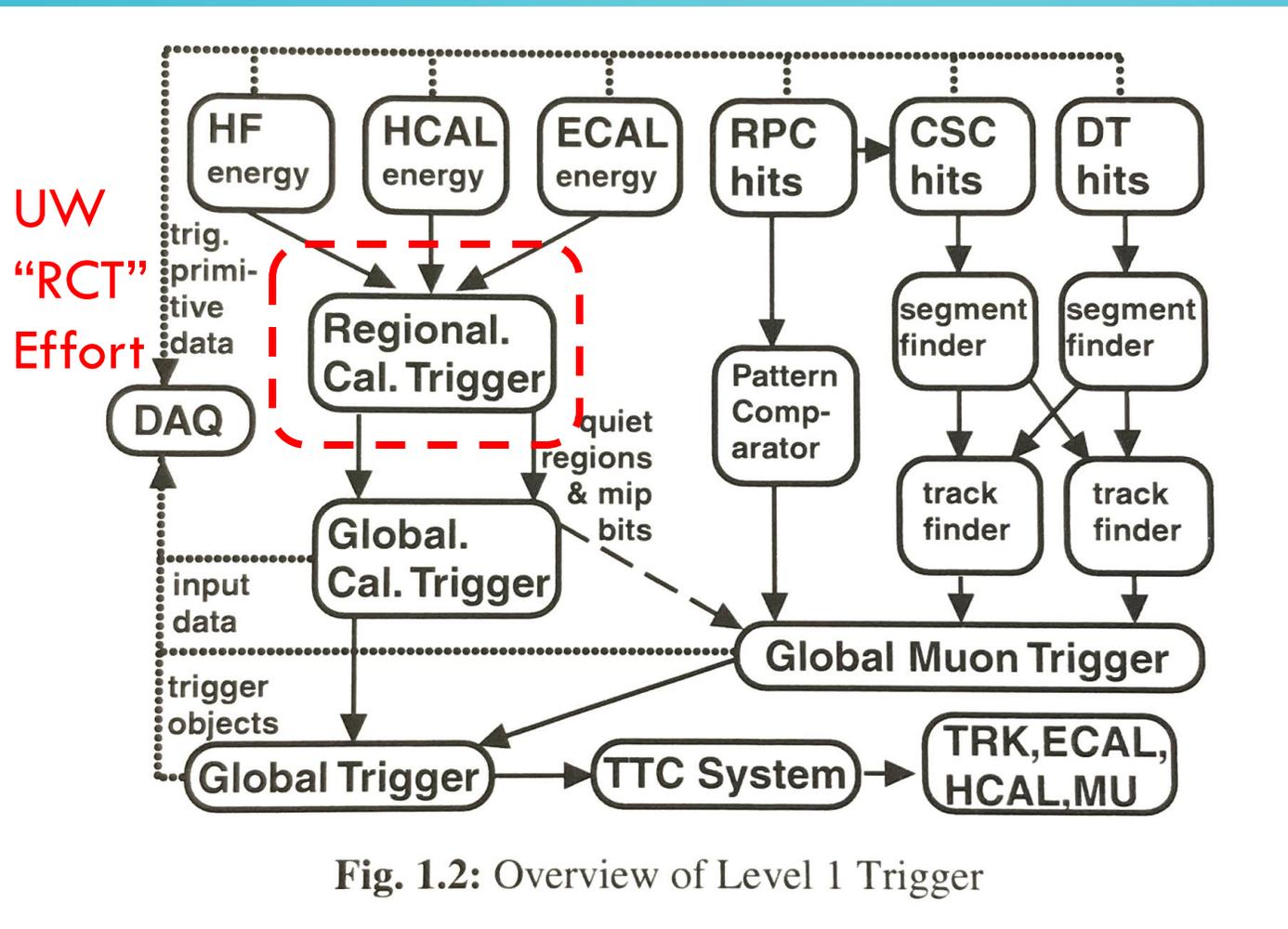
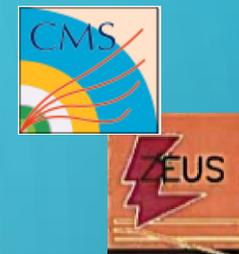


Fig. 1.2: Overview of Level 1 Trigger

But one major missing ingredient: no inner tracking at L1. Makes trigger job that much harder compared to earlier experiments. e.g. Muon momentum must be measured in the magnet yoke. No electron/photon discrimination.

SILICON TRACKING TO BE ADDED FOR HLLHC



SLHC Trigger & DAQ



LHC Electronics Workshop

Wesley H. Smith

U. Wisconsin - Madison

September 14, 2004



Outline:

Impact of Luminosity up to 10^{35}

Trigger Requirements

Calorimeter, Muon & Tracking Triggers

DAQ requirements & upgrades

R&D Technologies

This talk is available on:

http://cmsdoc.cern.ch/cms/TRIDAS/tr/0409/Smith_SLHC_LECC04.pdf

W. Smith, U. Wisconsin, LECC Workshop, September 15, 2004

SLHC Trigger & DAQ - 1

Wesley was already thinking about addressing this limitation as early as 2004



CMS SLHC L-1 Tracking Trigger

Ideas & Implications for L-1



Additional Component at Level-1

- **Actually, CMS already has a L-1 Tracking Trigger**
 - Pixel z-vertex in $\Delta\eta \times \Delta\phi$ bins can reject jets from pile-up
- **Could provide outer stub and inner track**
 - Combine with cal at L-1 to reject π^0 electron candidates
 - Reject jets from other crossings by z-vertex
 - Reduce accidentals and wrong crossings in muon system
 - Provide sharp P_T threshold in muon trigger at high P_T
- **Cal & Muon L-1 must produce output with suitable granularity & info. to combine with L-1 tracking trigger**
 - Also need to produce hardware to make combinations

Move some HLT algorithms into L-1 or design new algorithms reflecting tracking trigger capabilities

W. Smith, U. Wisconsin, LECC Workshop, September 15, 2004

SLHC Trigger & DAQ - 17

WESLEY WAS THE CMS L1 TRIGGER MANAGER SINCE THE EARLIEST DAYS



TRIDAS MINUTES 951108 - Trid x New Tab
Not Secure | cmsdoc.cern.ch/doc/tridas/minutes/951108

CMS DAQ MEETING, NOV 9 1995 at CERN - [Sergio Cittolin](#)

| | |
|---|--------------------------------|
| FrontEnd Driver (FED) Visual HDL model | A. Racz - 680kb, 20 Mb ps file |
| FrontEnd Logical model (FEL) | JF. Gillot |
| Status of FED developments | B. Halsall |
| Status of Dual Port Memory developments | A. Fucci |
| Status of EPFL ATM developments | A. Wiesel |
| Embedded systems and development tools | D. Samyn |
| PPC developments at H1 | B. Haynes |
| EuroBall FCS event builder status | G. Maron |
| ALICE prototype plans | S. Vascotto |
| US prototype plans | P. Sphicas |
| CMS prototype plans | S. Cittolin |

CMS TRIGGER MEETING NOV 10, 1995 at CERN - [Wesley Smith](#)

Calorimeter Trigger

| | |
|--|--|
| Calorimeter trigger performance on physics signals | S. Dasu |
| CMSIM study of electron trigger | C. Lourenco |
| CMSIM study of missing Et and tau trigger | A. Nikitenko |
| Trigger studies with CMSIM | G. Heath |
| Status of trigger primitive extraction | Ph. Bussone - page 2 - 3 - 4 |
| Calorimeter trigger ASIC and backplane update | W. Smith |
| Progress report on global calorimeter trigger | U. Schafer |

Muon Trigger

| | |
|--|--|
| B.x. identification with MF1 test beam data | V. Karjavin |
| 1/2 strip resolution with MF1 test beam data | P. Moissenz |
| Status of the DT trigger | Padova |
| Feasibility study of PAC trigger ASIC | Z. Jaworski |
| Status of the PACT test bench construction | I.M. Kudla - 1.6 Mb |
| Status of the CSC trigger | J. Hauser |
| Progress on DT/CSC Track Finder simulation | T. Wildschek |
| Progress on DT/CSC Track Finder design | A. Kluge - link to private files |
| Muon Trigger Overview | G. Wrochna |

Global Trigger

| | |
|---------------------------------|-----------|
| Global Muon and Level 1 Trigger | C. Wulz |
| TTC System | B. Taylor |

=====
docarchive 1.52 - /doc/tridas/minutes/951108 - 95/12/19 - 01:17:03
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Links to meetings still valid even after 24 years!

I JOINED THE PROJECT IN 1998



CMS Trigger Meeting April 27, 1998 New Tab

Not Secure | cmsdoc.cern.ch/~wsmith/Agenda498.html

TriDAS
Trigger and Data Acquisition Systems

[Previous Meeting](#) [Next Meeting](#) [TriDAS Home](#) [CMSdoc Home](#)

1998 Trigger Progress Report

Review of Cal & Global Triggers

Monday April 27, CERN

Calorimeter Trigger:

- [Review of Trigger Primitives -- J. Varela](#)
- [Review of Regional Trigger Hardware -- W. Smith](#)
- [Review of Regional Trigger Simulation -- W. Badgett](#)
- [Review of Global Calorimeter Trigger -- G. Heath](#)
- [Readout of Calorimeter Trigger Data -- G. Varner](#)
- [Summary of Milestones, Schedule, Cost -- J. Varela](#)

Global:

- [Status of Global Trigger - A.Taurok](#)

Synchronization Discussion:

- [Synchronization Issues -- W. Smith](#)

Review of Muon Trigger

Tuesday, April 28, CERN

Track-Finder:

- [Track Finder - J. Ero](#)
- [Track Finder synchronization issues - F. Szoncsó](#)
- [Track-Finding in rz-projection - M. Kloimweider](#)

CSC:

- [Trigger Primitive Generation/Processing - P.Padley](#)
- [Sector Processing & Track-Finding - D. Acosta](#)

Drift Tube:

- [Status of Trigger Server project - F. Odorici](#)

RPC:

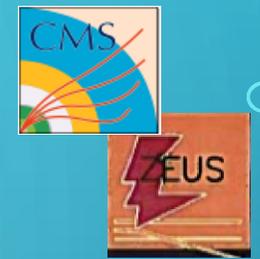
- [RPC PACT status & progress report - I.M.Kudla](#)
- [RPC schedule, project organization - J.Krolkowski](#)

Summary:

- [Summary & Milestones - G. Wrochna](#)

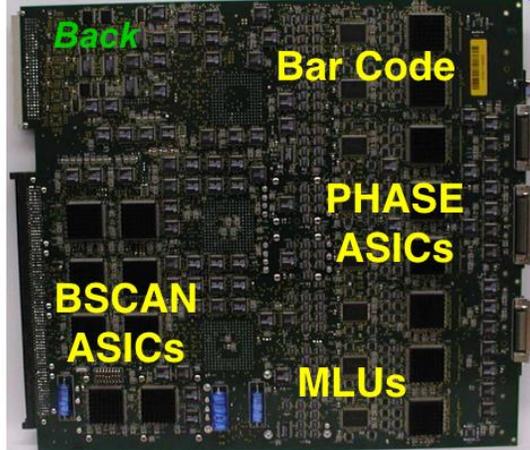
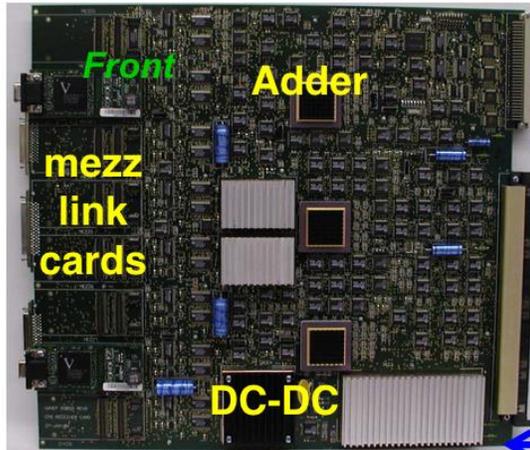


TYPICAL WESLEY SLIDE



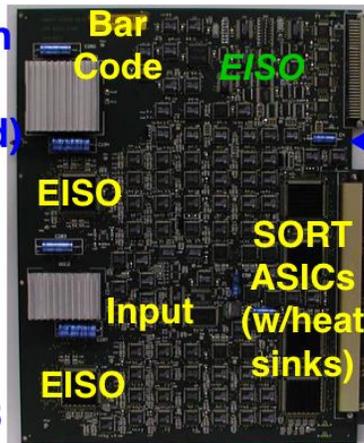
Regional Cal. Trigger Milestone: Major Production Complete

Receiver Card:



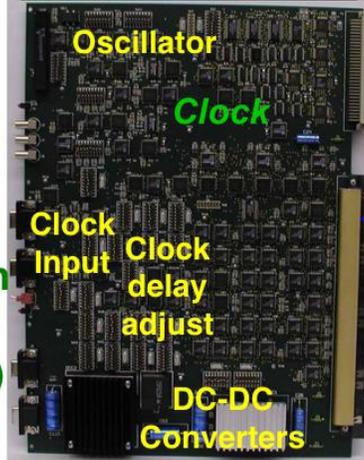
Electron Isolation & Clock:

fraction tested (needed)



124/153 tested (126)

(27/28 Custom Backpl Tested) (18)

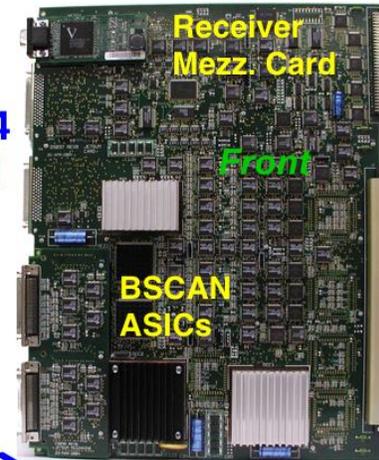


153/154 Tested (126)

3/25 tested (18)

7/25 tested (18)

Jet/Summary:



Always busy, with many, many acronyms!

Note the heavy use of ASICs, a product of the earlier SSC and HERA calorimeter trigger work

TYPICAL WESLEY TALK



17:15

Trigger

Speaker: Wesley Smith (University of Wisconsin)

15m



Always at a high rate 😊

Slides



1 Trigger Status
2 Trigger Integration Activities
3 Trigger Integration Progress
4 ECAL, HCAL, Regional Calorimeter Trigger Integration
5 SLB Synchronization in H4 Beam
6 Trigger in MTCC
7 Trigger Timing & Control in MTCC
8 Regional Calorimeter Trigger & HCAL in MTCC
9 Results from MTCC Phase 2
10 DT Trigger GB Setup for MTCC
11 DT MTCC Muon Trigger
12 CSC Trigger in MTCC
13 Full RPC Electronics Chain in MTCC
14 RPC PAC Trigger in MTCC 2
15 RPC & CSC MTCC Muon Triggers
16 Selected MTCC Muon Trigger Results: Example of DT & CSC
17 Selected MTCC Muon Trigger Results: Coincidence of DT and CSC Trigger
18 Event display of DT & RPC
19 ECAL TPC: TCC Barrel prodtest
20 RCT Installation in USC55
21 Global Cal Trigger Source Card
22 GCT Leaf Card Prototype Testing
23 GCT Concentrator Card Prototype
24 Global Trigger in MTCC Phase 2
25 Trigger Supervisor in MTCC
26 Beam Scintillation Counter
27 Trigger Installation Schedules
28 Online Selection & Trigger Physics
29 Example: Min-Bias Trigger
30 Trigger Planning & Coordination
31 Trigger Meeting in 2007
32 Summary - Trigger

FIRST CMS LEVEL-1 TRIGGER ELECTRONICS



- RCT was implemented in 18 VME crates
 - Also five high-speed custom GaAs ASICs were designed and manufactured by Vitesse: a phase ASIC, an adder ASIC, a boundary scan ASIC, a sort ASIC, and an electron isolation ASIC.

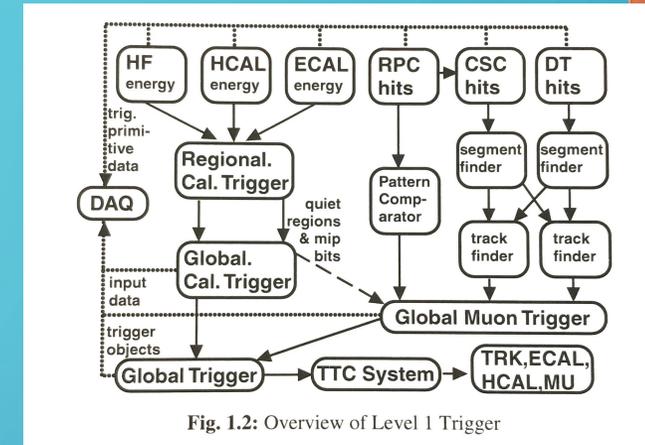
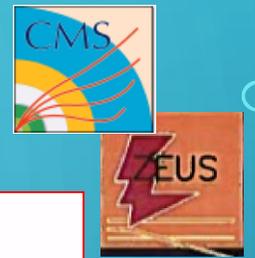


Fig. 1.2: Overview of Level 1 Trigger

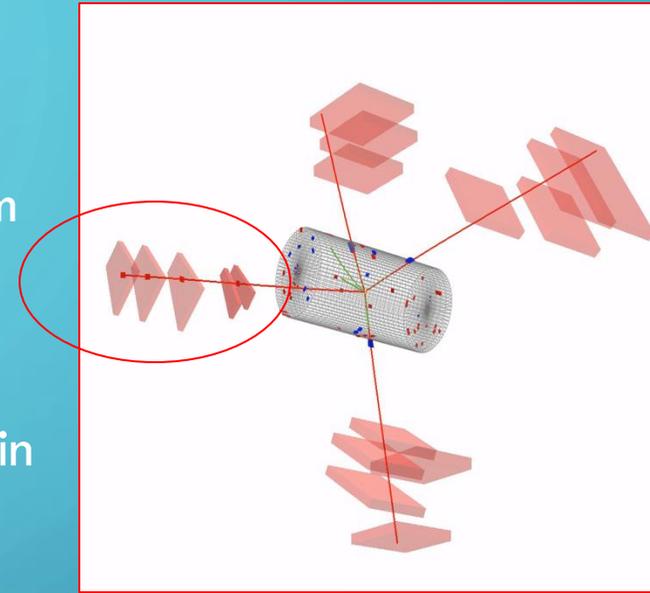
- The muon trigger subsystems, such as the CSC Track-Finder, typically occupied 1-2 VME crates each and utilized Xilinx FPGAs and a few ASICs for pattern finding
- The **FPGA revolution was taking hold**, as well as high-speed **optical links** for data transmission (~ 1 Gbps)

LEVEL-1 TRIGGER ALGORITHMS



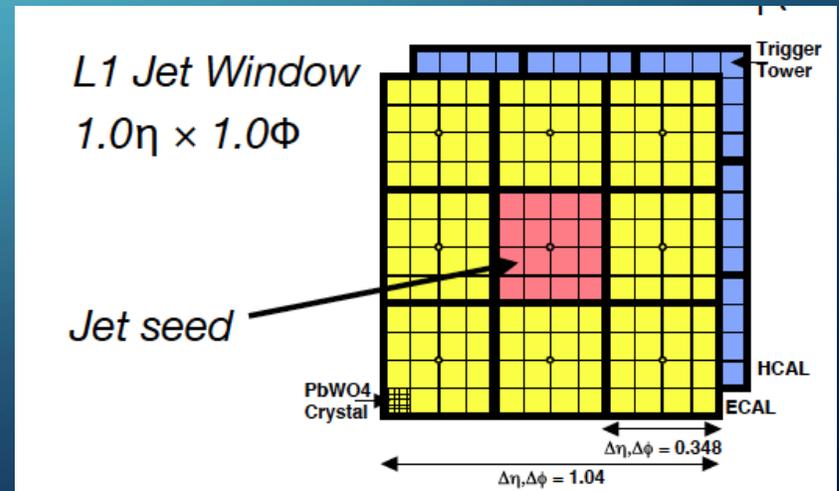
- Muon Track Finding

- Extrapolation-based matching of segments from one muon detector station to another (aka “Tracklet”)
- Momentum assignment based on the deflection in φ from one station to the next from the fringe field in the yoke

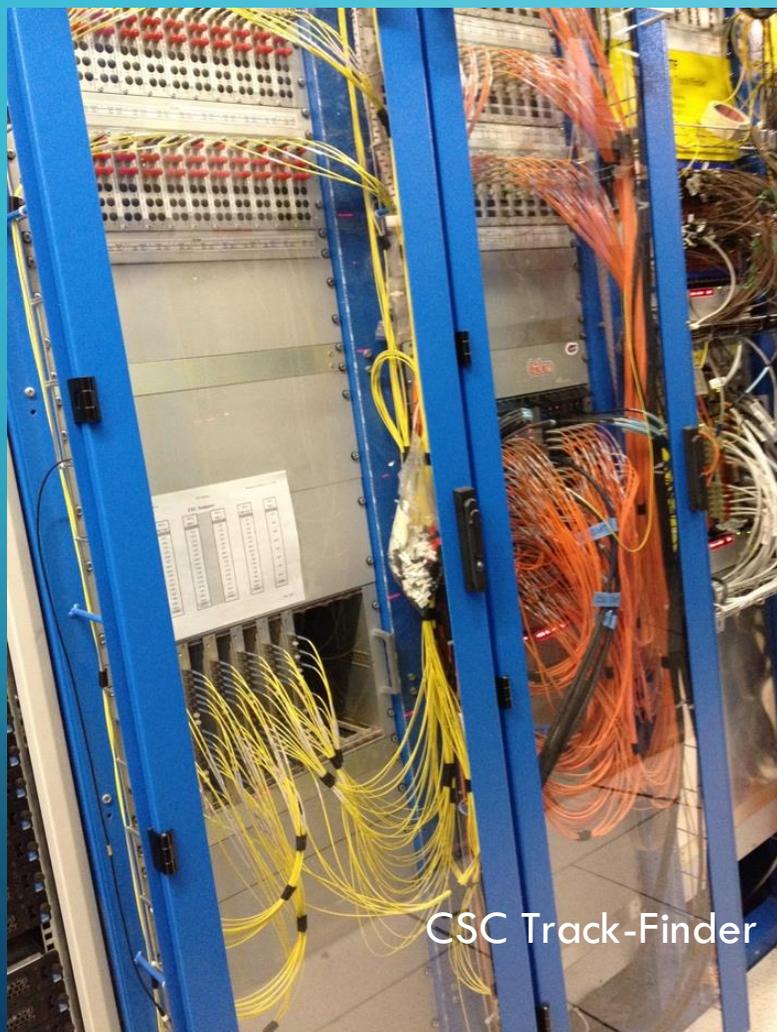


- Electron, tau, and jet clustering

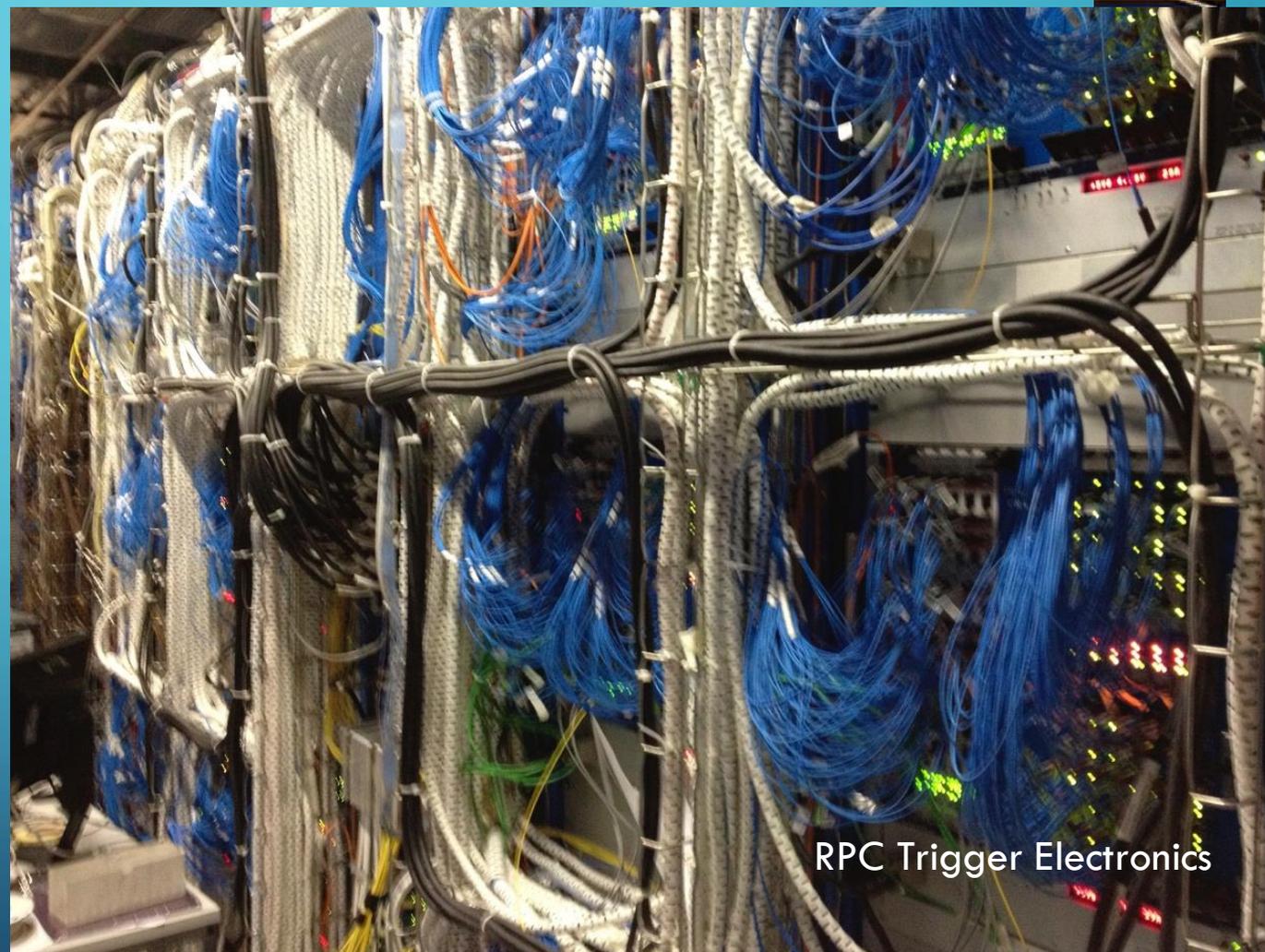
- Each TT has $\Delta\varphi\Delta\eta = 0.0875 \times 0.0875$
- Electron candidates (isolated and nonisolated) found in 4x4 TT regions
- Sliding window for jets across 4x4 TT regions



CMS LEVEL-1 TRIGGER SYSTEM INSTALLED

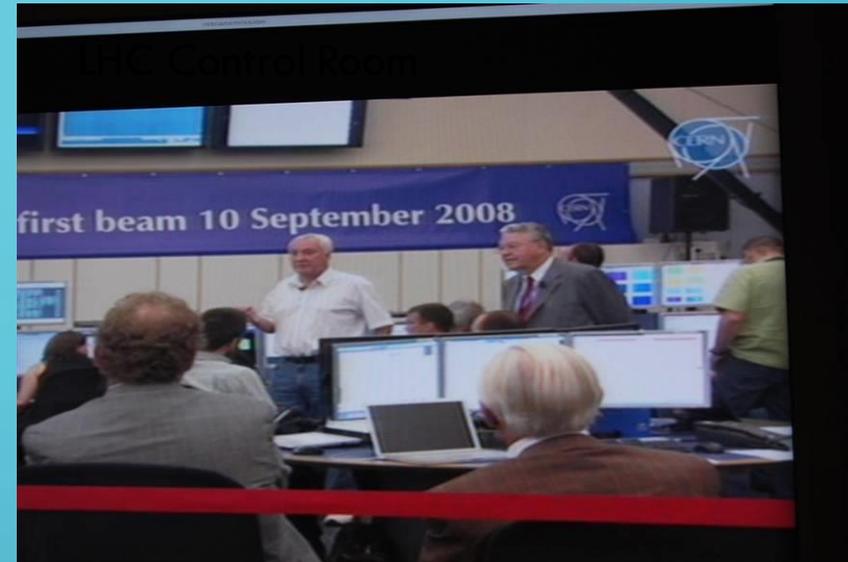


CSC Track-Finder



RPC Trigger Electronics

READY FOR FIRST LHC BEAMS IN 2008



About a week later we were 5 days away from first pp collisions, and yet CMS had no HLT menu yet!



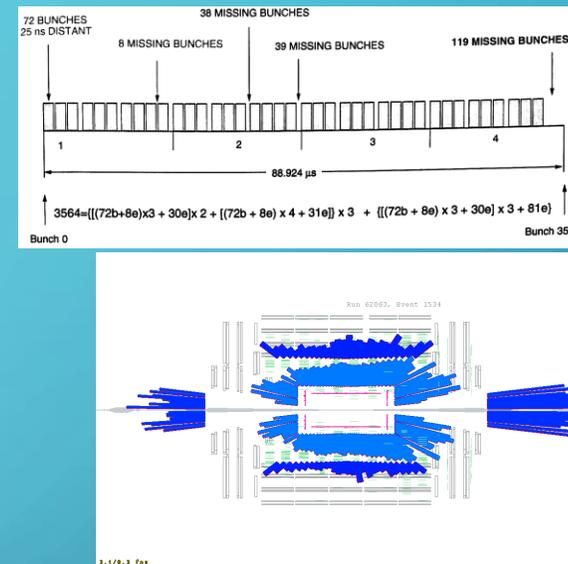
But we did take the opportunity to upgrade the FPGAs on the endcap muon trigger at least to add more margin!

Sadly, the LHC suffered a major malfunction on a black Friday, September 19, 2008, delaying things by more than a year and forcing us to lower the beam energy

SOME CHALLENGES THAT REQUIRE AGILITY

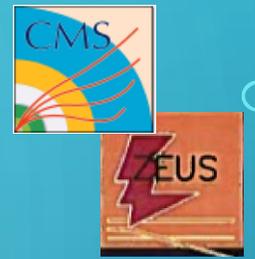


- Synchronization of millions of channels
 - Relative synchronization of neighboring detectors
 - Absolute synchronization using LHC bunch structure
 - LHC beam collimator “splash” events !
- ECAL APD spikes from neutral hadrons
 - Jeopardized electron trigger with high rates!
 - Fortunately crystal size is narrow enough to lead to energy sharing among neighbors for real electrons → spike suppression algorithm
- Trigger prefiring
 - Calorimeters trigger primitives can fire early, causing us to read wrong BX for DAQ
 - Solution: veto unfilled colliding bunches
 - Problem: how to trigger on possible slow HSCPs?
 - Solution 2: Latch and hold RPC trigger hits for 2 BX (50 ns)

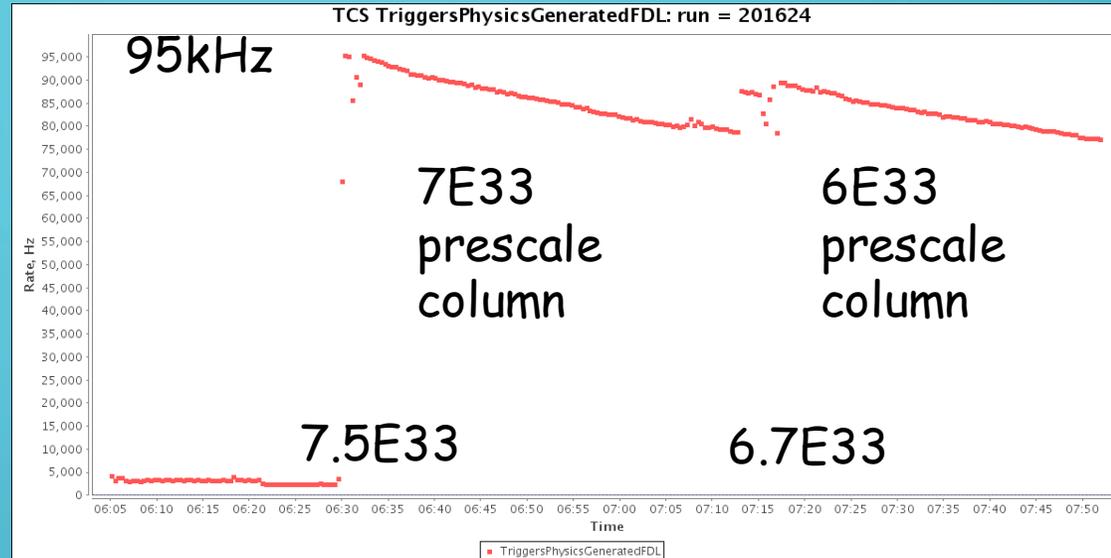


Wesley's suggestion

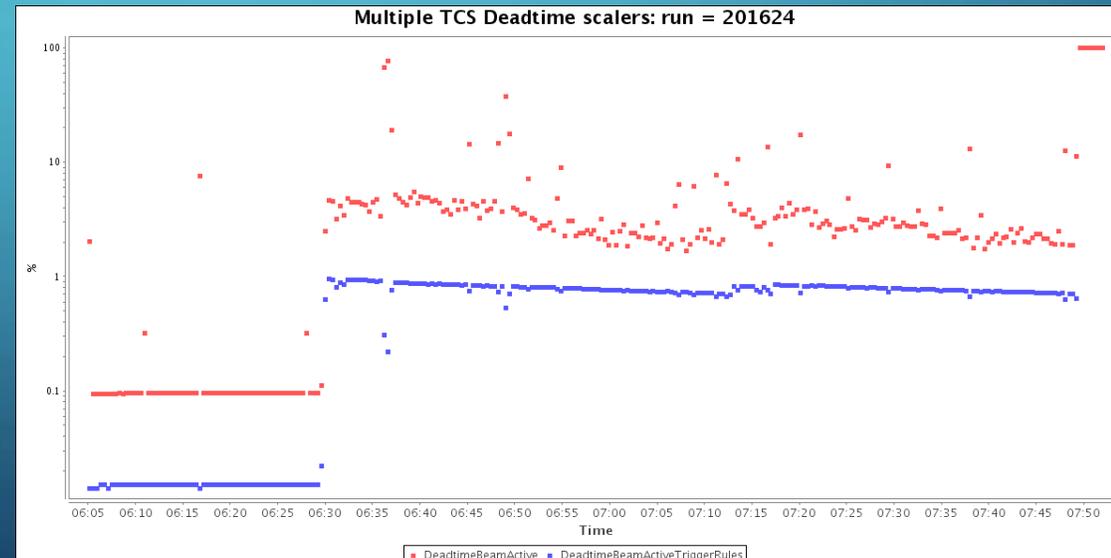
BUT EVENTUALLY EVERYTHING WORKED!



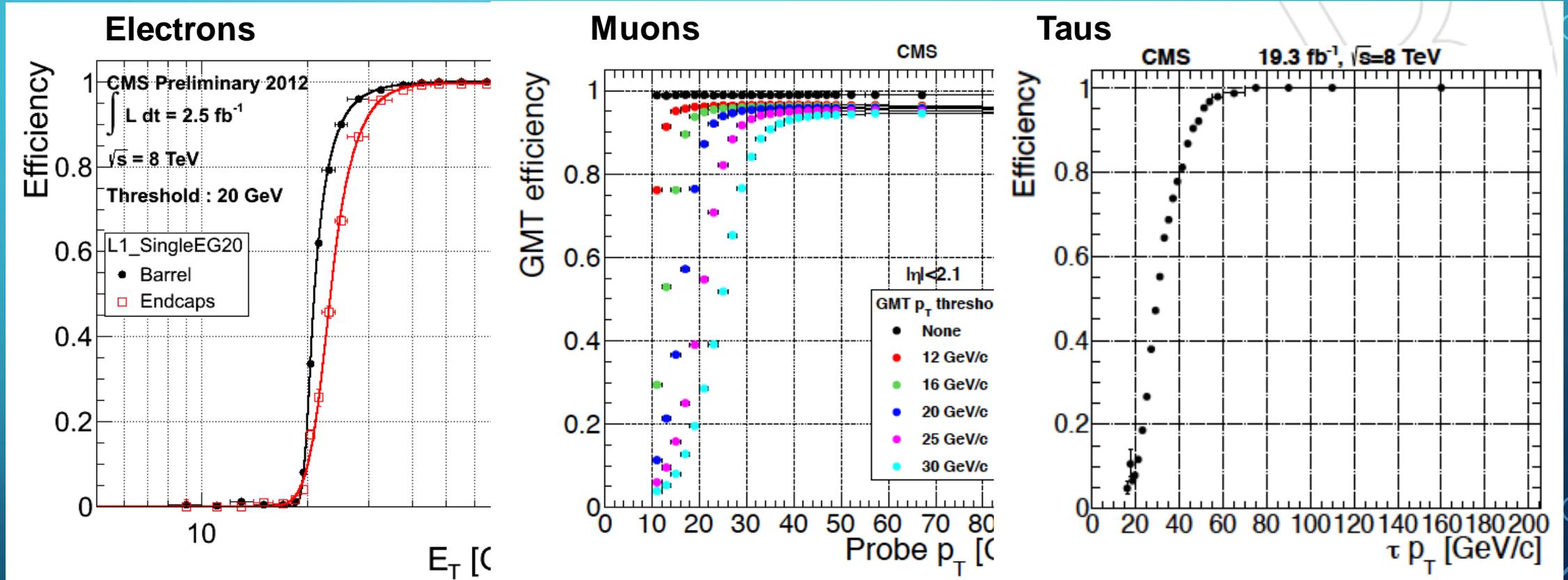
- L1 rates happily cruising at near 100 kHz !
 - Fill from 2012



- Low deadtime
 - Trigger control and throttling system, and DAQ, all working!



GOOD EFFICIENCY FOR PHYSICS!



IN 2012: DISCOVERY OF THE HIGGS

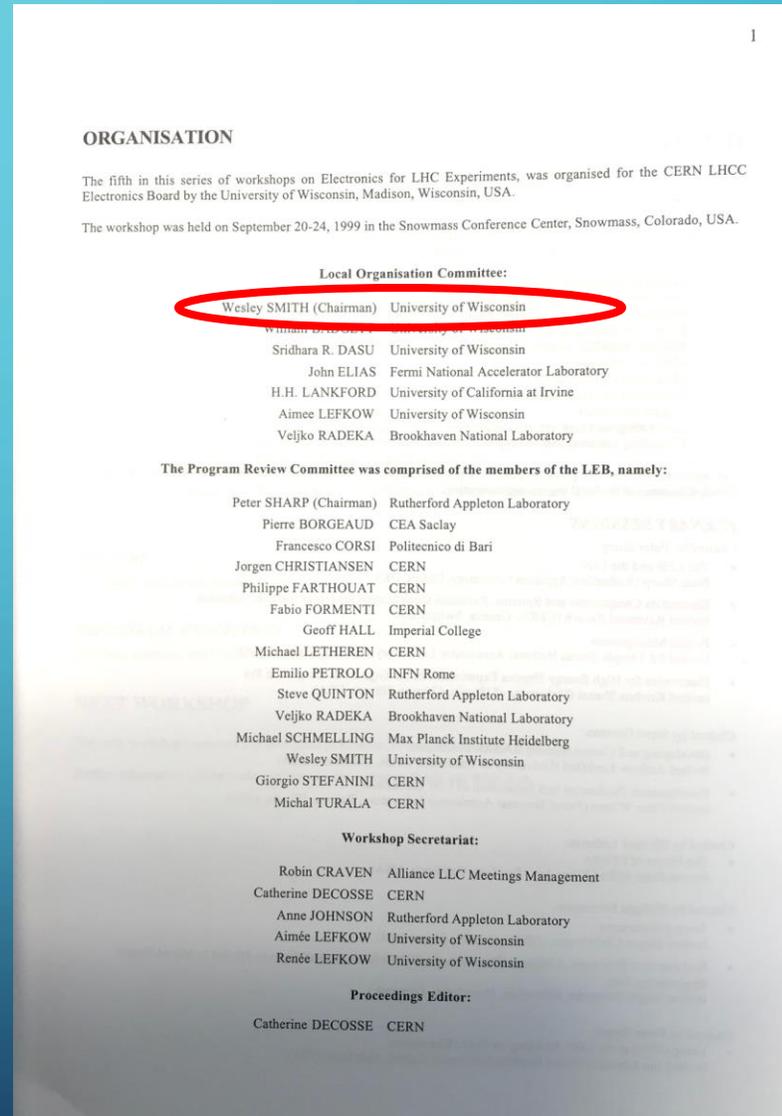
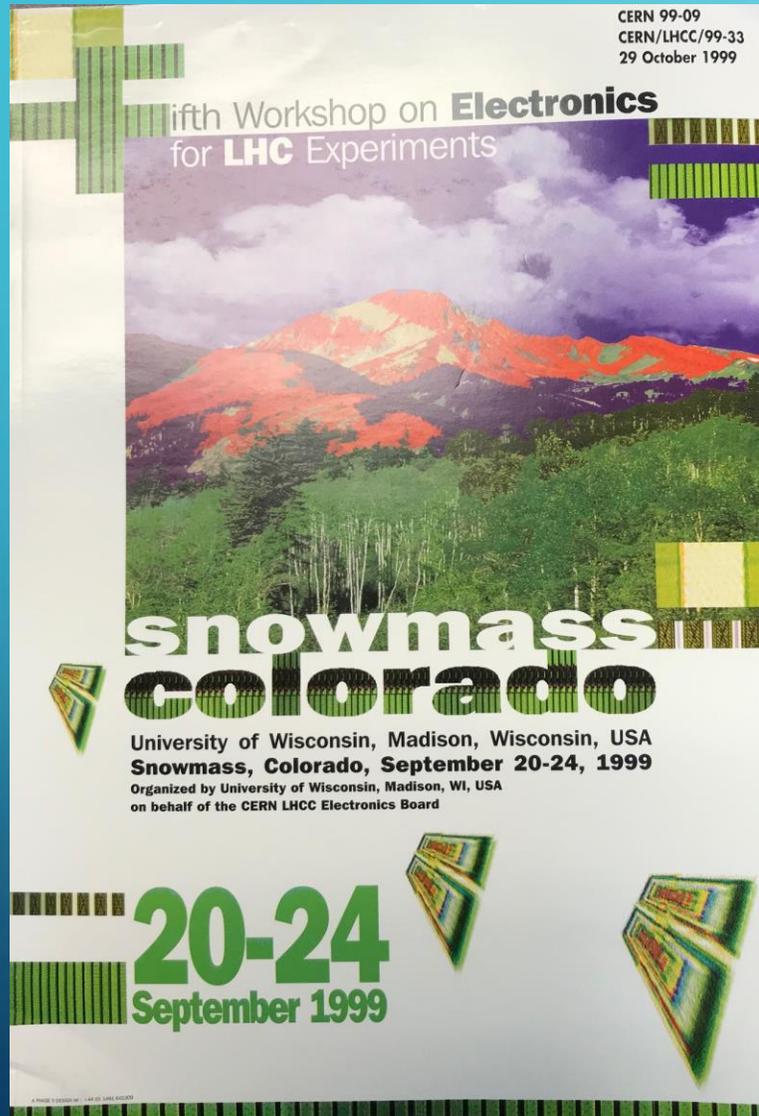
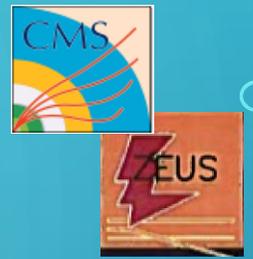


François Englert and Peter Higgs
Photo: © CERN

2013 Nobel Prize in Physics



A LEADER IN LHC ELECTRONICS DEVELOPMENT



LEB Workshops,
now TWEPP

LHC ELECTRONICS WORKSHOPS



REASONS FOR AN UPGRADE: PHASE-1



CSCTF VME processor

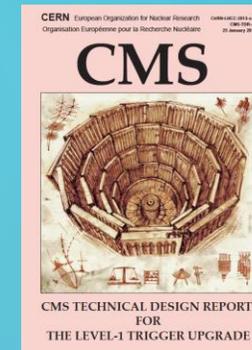
The DTTF
"Green Salad"



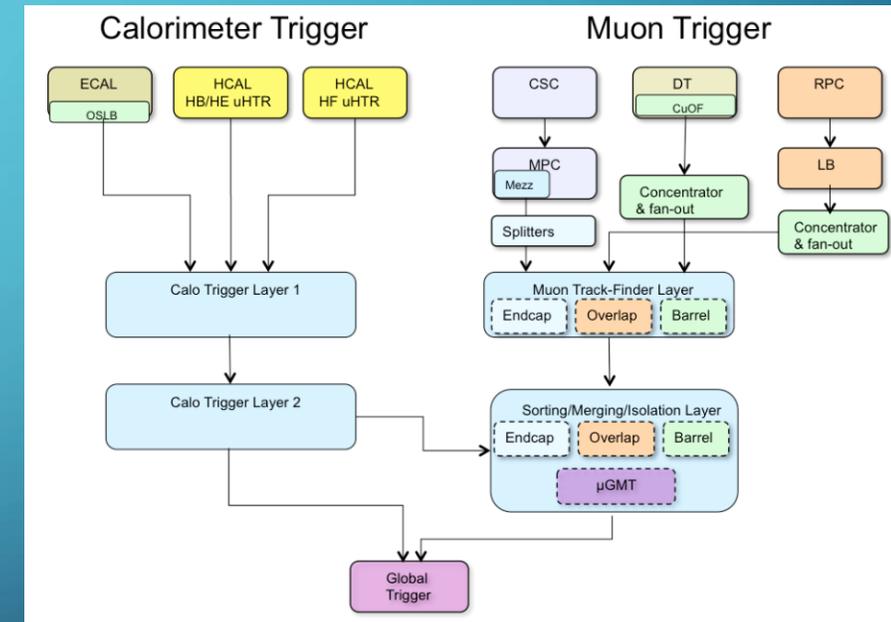
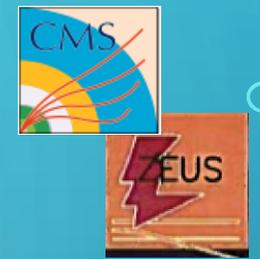
- LHC Run 2 anticipates:
luminosity and pileup twice higher than design!
- ASICs cannot be reprogrammed
- Older FPGAs near capacity, and memory look-up tables small
- Lots of copper cabling (data volume and format fixed)
- Large, fragile VME cards

PHASE-1 TRIGGER UPGRADE

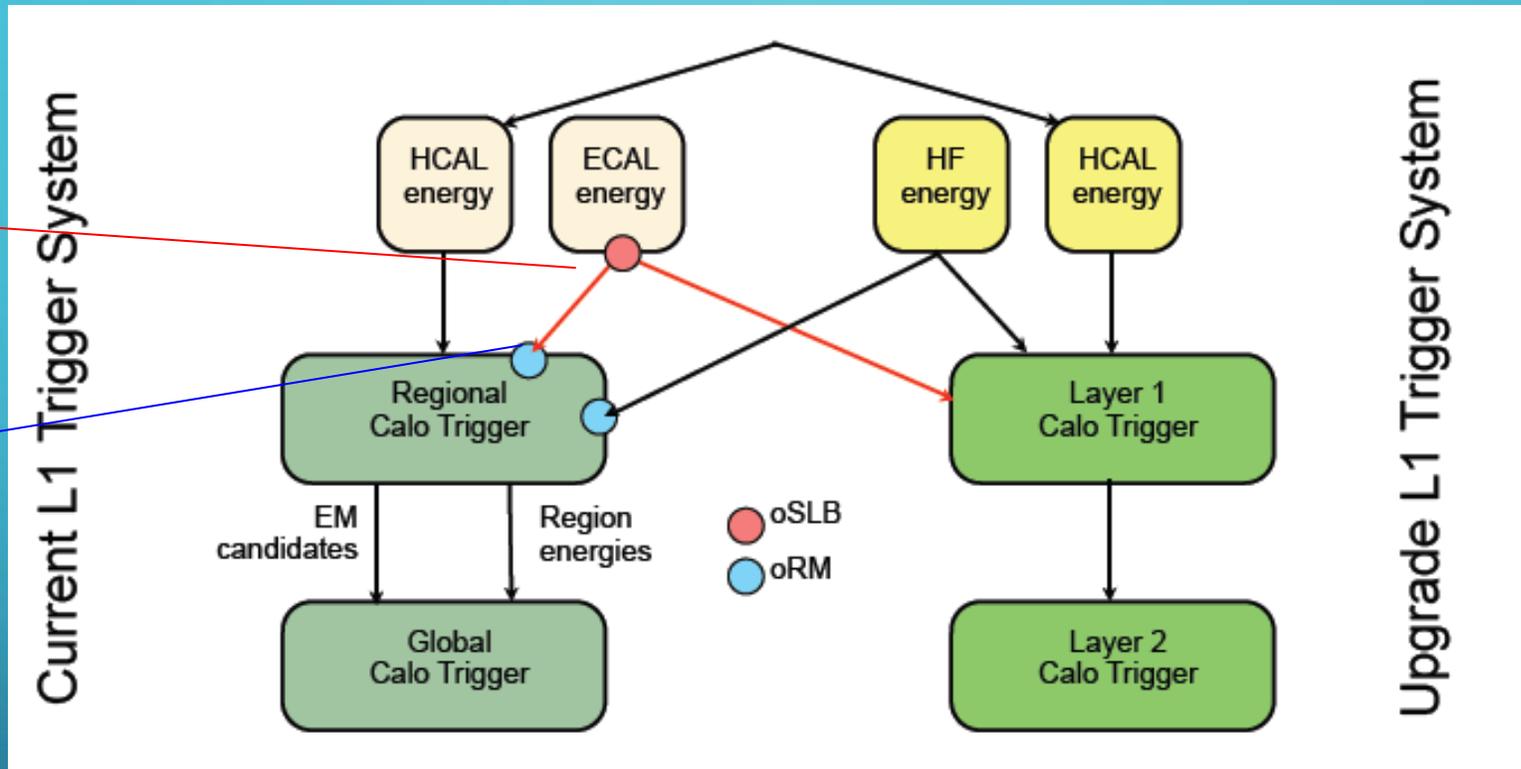
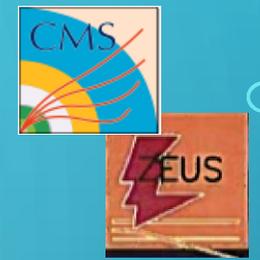
- Mitigate rates by improving:
 - e/γ isolation
 - τ id
 - muon p_T resolution and muon isolation
 - jets with PU subtraction
 - L1 menu sophistication
- Increase system **flexibility** with higher bandwidth optical links (~ 10 Gbps) and larger Xilinx FPGAs
- **Standardize** on the μ TCA telecomm standard in CMS (something Wesley started with a Los Alamos connection)



TDR in 2013



CALO TRIGGER TRANSITION TO PHASE-1



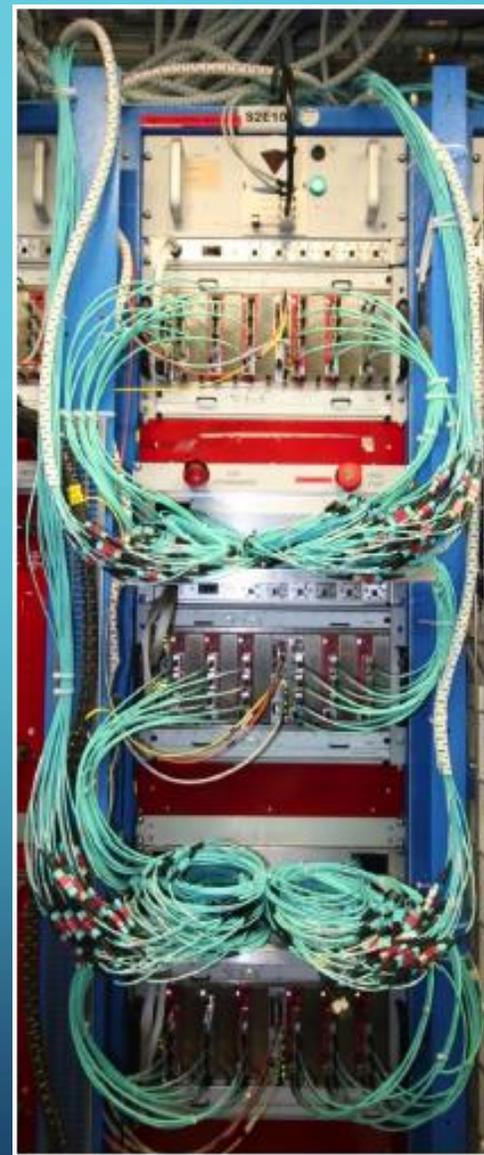
Wesley and Wisconsin had a good plan here, including also a “Stage-1” early upgrade deployment in 2015

- Important to build and **commission upgrade in parallel** with current trigger system to safeguard physics, decouple from LHC schedule
 - e.g. Duplicate ECAL signals with active optical components, and split HCAL optical inputs to HCAL back-end electronics



PHASE-1 TRIGGER HARDWARE

- Thankfully it too worked!
- But maybe only because Wesley ensured enough latency margin in the overall trigger design (we used every last BX...)

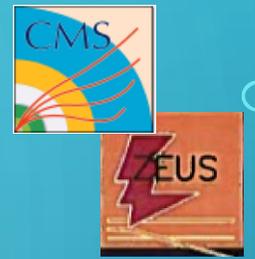


CTP7 rack for
Calo Layer-1



MTF7 rack for
EMTF

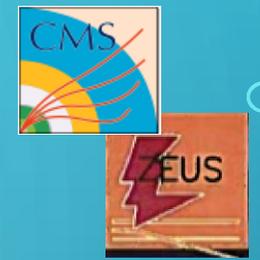
ORIGINAL RCT RECENTLY DECOMMISSIONED



- The original Regional Calorimeter Trigger now decommissioned in 2019, as it has been replaced by the Phase-1 upgrade in 2016



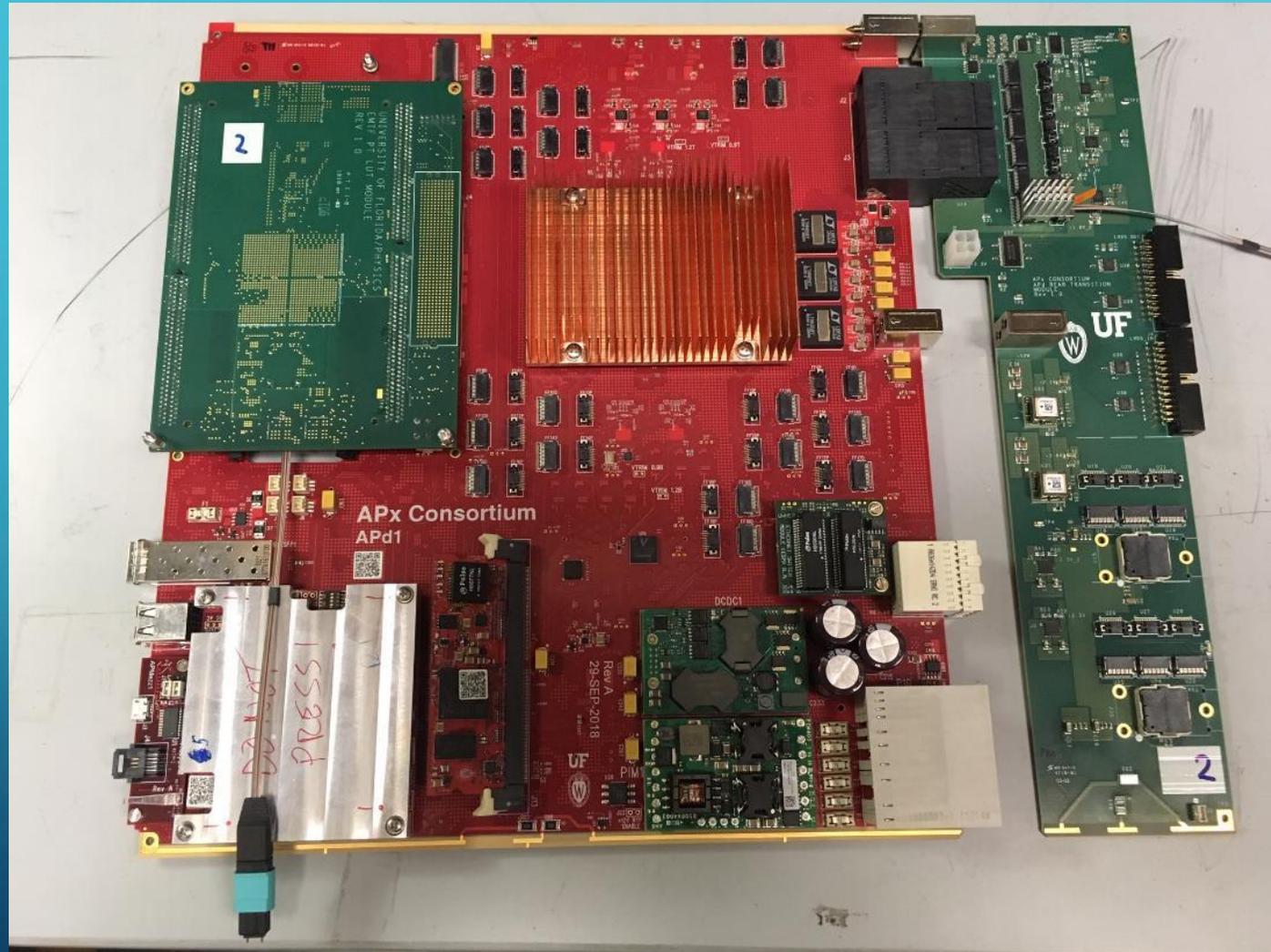
NEXT GENERATION L1 TRIGGER FOR HL LHC



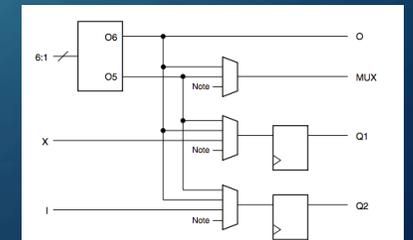
- Incorporation of tracking at Level-1 from the silicon tracker
 - Major missing ingredient!
- Correlation of tracks with other Level-1 objects
 - Better charged lepton ID, refine (muon) momentum, assign jet vertex, determine primary vertex, provide track-based isolation ...
- Introduction of crystal granularity at Level-1 for ECAL barrel
 - $\Delta\phi\Delta\eta = 0.0175 \times 0.0175$ vs. 0.0875×0.0875
 - Better spike rejection and EM shower identification
- Incorporation of Phase-2 forward muon detectors into muon trigger
 - Increased redundancy, more bending angles
- Trigger rates up to 750 kHz @ Level-1, 7.5 kHz @ HLT (vs. 100 kHz and 1 kHz today)
- Level-1 trigger latency of 12.5 μ s (vs. 4.0 μ s today)
 - Allow time for additional processing (Track Trigger, Correlation)

Foresight to push both for tracking @ L1, and increased output bandwidth to better balance L1 and HLT

AND WE'RE ON OUR WAY!



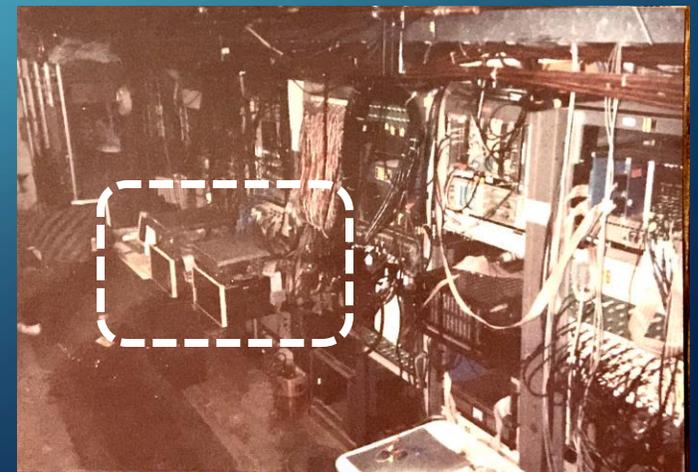
- APx R&D:
- I/O: 25 terabits/sec
- 2.5 million logic cells



A LARGE LEAP FROM THE PAST



- A far cry from the ~ 32 AND gates that I programmed into a PAL for the Csl trigger logic of the SLAC TPC/2Gamma experiment in 1988
- Or the wire-wrapped trigger logic for the CLEO-II experiment...



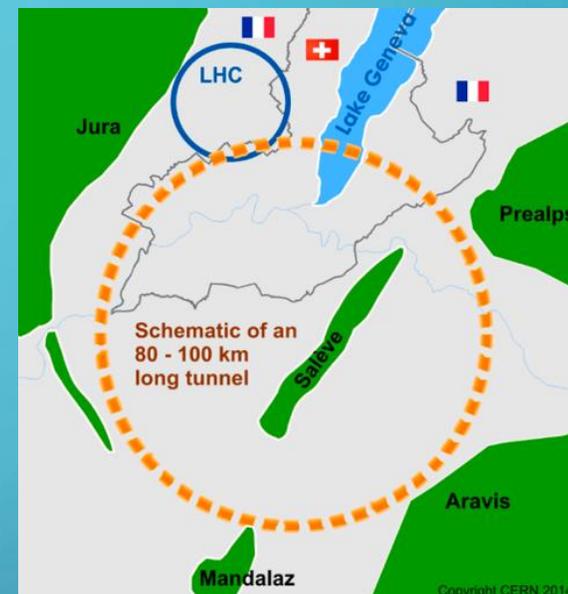
FUTURE CIRCULAR COLLIDER (HADRON)



But APD may be just as primitive compared to a system for a FCC, 40+ years from now !

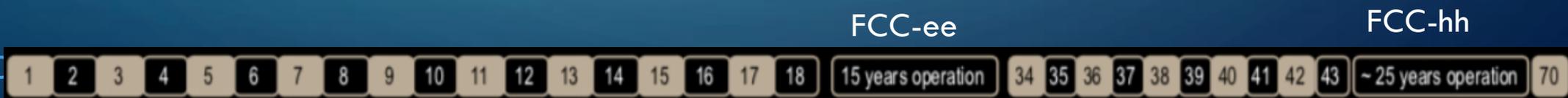
- Goals:

- Higher energy: ~ 100 TeV
 - Explore high energy frontier
- Higher luminosity: $5-30 \times 10^{34}$ Hz/cm²
 - High precision, e.g. Higgs boson couplings



- Trigger Challenges:

- Pileup: $O(1000)$ pp collisions per beam crossing (20X more than LHC)
- Higher detector channel count from increased granularity
- Radiation levels in tracking volume





TRAVEL & EATING

PIZZA IN MEYRIN



VOLCANOS



2010 eruptions of Eyjafjallajökull



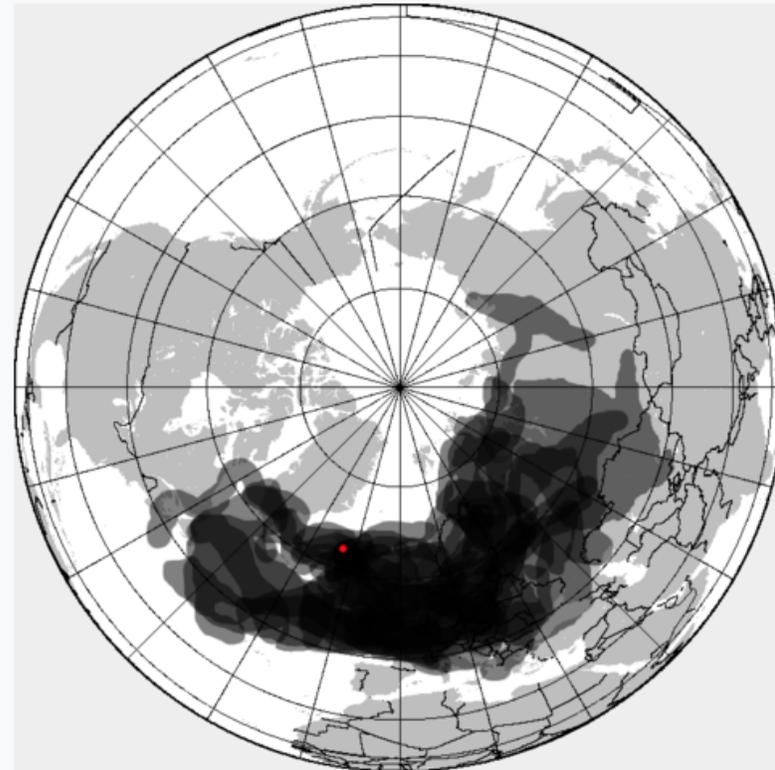
Volcano plume on 18 April 2010

| | |
|-------------|---|
| Date | 20 March – 23 June 2010 |
| Type | Strombolian and Vulcanian eruption phases |

Wikipedia

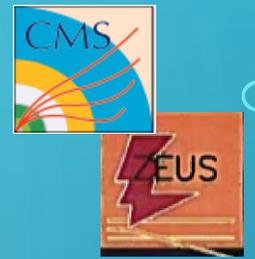
Kept us a bit longer than anticipated at CERN

Impact large-scale disruption to air travel, smaller effects on farming in Iceland



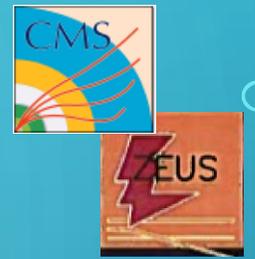
Composite map of the volcanic ash cloud spanning 14–25 April 2010

IN CONCLUSION



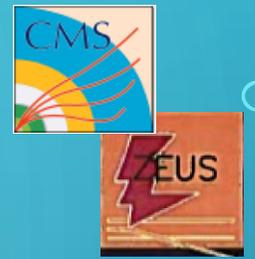
- “So long, and thanks for all the triggers!”
- Your legacy will always be a part of the experiments, and the high-energy physics community
- You set a good example of taking the correct, hard decisions, and fighting to achieve them (triggers, physics, management, etc.)
- Thanks for all the opportunities!
- I wish you well in a hard-earned retirement

THANKS



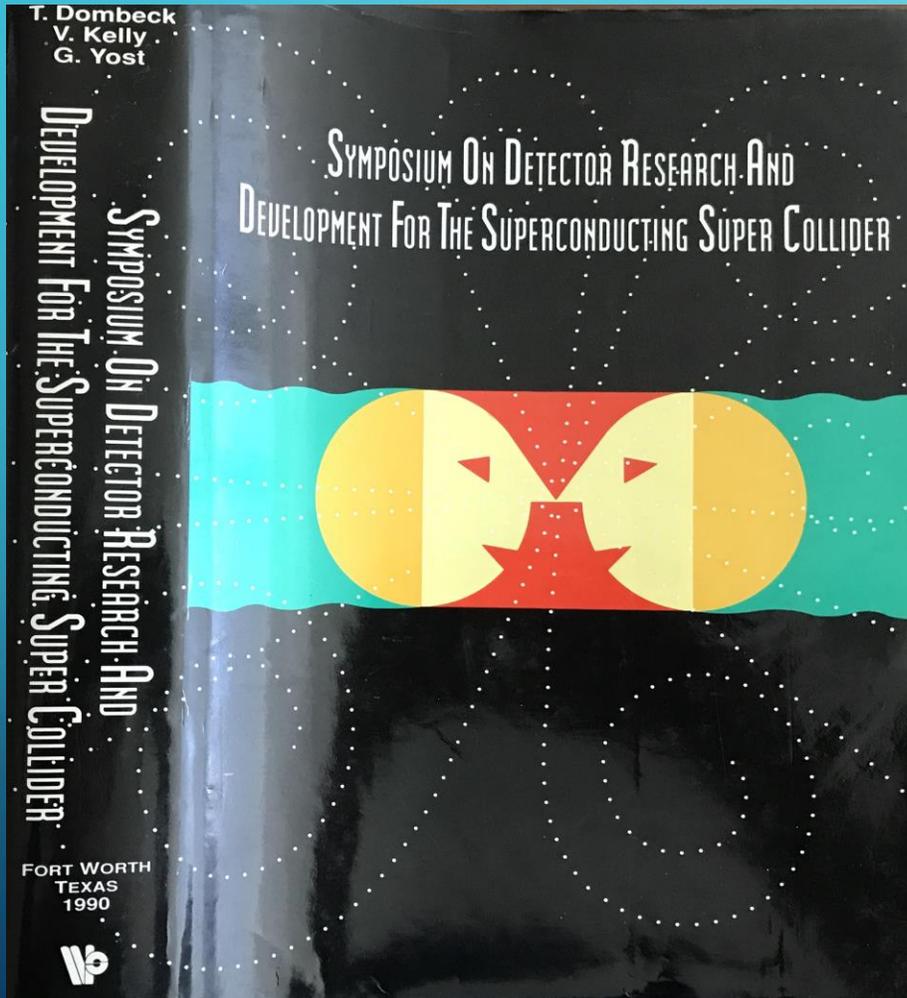
- To Stan Durkin and Ben Bylsma for help with ZEUS trigger info

AN ASIDE ON KINEMATICS AT COLLIDERS



- Energy and momentum is always conserved in general, but observed quantities may not because of particles escaping down the beam pipe or because of neutrinos (and neutralinos?)
- e^+e^- colliders
 - Total observed energy and momentum is conserved for annihilation processes (thus provides a \sqrt{s} constraint)
- Hadron colliders
 - Observed longitudinal momentum (p_z) is not conserved in hadron-hadron colliders, because of the unknown parton momentum fraction x in each struck hadron
 - Transverse momentum is. Unbalanced attributed to MET from unmeasured particles
- $e p$ colliders
 - While p_z is not conserved, $E - p_z = 2E_e$ is for an ep collider. Provides another kinematic constraint handle that pp colliders do not have

SSC R&D SYMPOSIUM, 1990



DESIGN OF READOUT ELECTRONICS FOR A SCINTILLATING PLATE CALORIMETER

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Abstract

We describe the progress made on the design of readout electronics for a compensating scintillator plate calorimeter.

INTRODUCTION

A scintillator calorimeter produces unique problems for the designer of readout electronics. On the one hand the narrow time structure of scintillator pulses, ~10 nsec, is well matched to the structure of the SSC and gives the hope of isolating information from individual beam crossings. On the other hand, the compensation mechanism and the need to broaden the pulse shape for use with analog signal sampling devices gives a somewhat wider time structure, ~50-100 nsec. Furthermore the granularity of such a device implies that the full energy of an electromagnetic shower may be totally contained within one readout channel. If the resolution of the electronics is not to compromise the intrinsic resolution of the calorimeter, assumed to be $\sigma/E = 15\%/E + 1\%$ (E in GeV), coverage of the full dynamic range (40,000:1) requires at least two 12-bit devices with 7 bits of overlap for a linear front-end electronics chain.

The positioning of the electronics also is a critical issue. At luminosities of $10^{32} \text{ cm}^{-2}\text{sec}^{-1}$, electronics placed on the calorimeter must withstand doses of at least 10^{16} neutrons/cm² and 2000 Rad per year at 90°.

In the past year, the scintillating calorimeter collaboration has begun studying these and related issues. Among the work reported below is: a study related to remote location of the calorimeter electronics, a comprehensive program to evaluate the properties of FADCs capable of operation at 60-80 MHz, design of an analog memory unit and development of a "benchmark system" to help evaluate components under development both within and outside our collaboration.

REMOVING OF ELECTRONICS

The advantages of locating a substantial fraction of the front-end electronics away from the calorimeter

include: accessibility and hence ease of maintenance and future upgrades, significantly reduced exposure to radiation and more space for cooling. The systems evaluated involve either using fiber optics for transmitting signals from phototransducers on the calorimeter to remote electronics, or bringing the scintillator light signals along fiber optic paths to remote phototransducers and electronics.

An investigation was made of the performance and cost of fiber optic links for sending analog data signals (and a possibly digitized trigger signal) from and digital control and clock signals to a multiplexed set of phototransducers. Analog bandwidths above 200 MHz and digital rates of up to 2 Gigabits/sec exist for such systems. The dominant cost in the alternative scheme of bringing the scintillator light away from the surface of the calorimeter is in the fiber itself. Long, low attenuation fibers are required and the total fiber length is in excess of 10,000 km. Low loss glass fibers are available, but the cost is prohibitive (\$3000/km). There also may be difficulty in bonding glass fibers to the wavelength shifter fibers of the calorimeter. Clear acrylic fibers are currently being evaluated as an alternative approach.

FADC EVALUATION

A systematic study of commercially available Flash A/D converters capable of 100 Megasample per second operation has begun [1]. Such FADCs could be used to digitize the phototransducer output for trigger purposes or could be used with a non-linear preamplifier as part of the data collection stream. (Development of such an ASIC preamplifier is part of a Fermilab effort.)

We have built a CAMAC based test bench controlled by a VAXstation 3100 for the testing of FADCs. Communication with the test bench components is via both SCSI and GPIB buses. Two special purpose programmable CAMAC boards have been built: one provides clock and trigger signals, the other interfaces to various evaluation boards. The clock/trigger board allows ten discrete frequencies in the range 20-140 MHz to be supplied to the FADC under test. The FADC board contains 1 kbyte of 12-bit memory to store the digitized data. FADCs with dynamic ranges up to 12-bits can be tested. (Minor modification of the clock/trigger board can extend the range of available clock frequencies to lower values.) The test procedures follow the guidelines given in IEEE Std-1057, "IEEE Trial-use Standard for Digitizing Waveform Recorders." Among the properties measured are gain, offset, differential and integral non-linearity, maximum static error, monotonicity, hysteresis, effective number of digitizing bits, signal-to-noise ratio, peak error, aperture uncertainty, settling times, etc. Table 1 gives preliminary results of some of these studies for three of the FADCs currently under test.

| | AD9002 | CXA1176 | CX20116 |
|-----------------------------------|----------------|--------------|---------|
| Flash ADC Manufacturer | Analog Devices | Sony | Sony |
| Advertised Maximum Rate (MSPS) | 125 | 300 | 110 |
| Clock Rate for Measurements (MHz) | 30.0 | 80.0 | 20.0 |
| Gain | | | |
| Static | 0.995 | 0.991 | 0.996 |
| Dynamic | 0.983 | 0.989 | 0.995 |
| Differential Non-Linearity | | | |
| Sine Wave | 0.300 | 1.000 | 0.800 |
| Triangle Wave | 0.297 | not measured | 0.559 |
| Integral Non-Linearity | 0.576 | 0.638 | 0.333 |
| Signal-to-Noise Ratio | 168.1 | 156.0 | 202.5 |
| Effective Number of Bits | 7.271 | 6.988 | 7.465 |

Table 1 - Preliminary Results from FADC Testing

ANALOG MEMORY

One possible scheme for collecting data from a scintillating calorimeter is given in Figure 1. In this scheme A/D conversion is done after two levels of triggering. This reduces the speed at which the conversion must be accomplished, but requires the data be stored in analog form for periods of up to 50 μsec . In addition if the storage is to be done on the outer surface of the calorimeter the analog memory units must be radiation hard. A VLSI chip to store analog signals from the calorimeter has been designed and is scheduled for submission to the MOSIS foundry in early November, 1990. The analog phototransducer output signals are

Figure 1 - Possible Readout Architecture