ASICs and Readout Basic Research Needs for Future Experimental HEP Detectors

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Long Term Needs to Maintain IC Development and Implementation

The most crucial aspect of maintaining US competitive edge in ASIC design for Instrumentation of HEP Detector systems is the support for and constituency of the future design teams.

These priorities Include:

- **Long term support for Design Engineers & Instrumentation Physicists**
- **Access to design and verification tools relevant to the complexity of designs**
- **Improvement of the eroding possibility for Multi-Institutional Collaboration**

Long Term Needs

Sustaining IC design workforce and IC design literacy among Physicists

Complex multi-functional ASICs will certainly be the common enabling experimental workhorse that drives the breakthrough potential of future High Energy Physics detector systems.

- **Physicists and Engineers need to work together with a common understanding of the state of the art of IC design and how it relates to our future detector systems. This affects all stages of ASIC design from the signal processing and readout architecture design to the evaluation and meaningful review of designs as they progress to the final review of functionality and the understanding of how to exploit the ASIC provided data.**

Means to sustain a work force and provide broad community understanding:

- **Entry Level ASIC training for grad students, post docs and interested University faculty could be provided by Labs hosting visitor positions offering ASIC design courses online with support from lab personnel and "hands on" experience. Encouragement might be offered in the form of ~10% expert salary coverage…**
- **DOE funded FOA's with a range of ASIC projects targeting next generation detector systems could community interest (and discretion) could be used to define which projects are funded.**

Long Term Needs

Access to future tools and processes:

Since inception In 1981 MOSIS supported by UC Southern Ca. provided foundry access to technology files and offered a wafer brokeraging service to many research groups including HEP.

- **In May 2019 MOSIS dropped support for research institutions leaving US HEP foundry support in limbo as MOSIS turned their attention to very expensive 22nm and smaller technology nodes.**
- **An Important positive result was that within a few months IMEC, a Belgium based microelectronics R&D group that also supports ASIC fabrication brokeraging services approached many US HEP groups to offer support for access to TSMC technology nodes at 180 through to 65nm.**

It appears that there are currently NO US commercial based ASIC fab companies that participate in supporting US HEP research initiatives.

- **It would be quite helpful to have funding and logistical support from DOE and other government Agencies to encourage US IC foundries to help with US research work in areas where custom IC's can lead to breakthrough discoveries.**

Long Term Needs

Multi-Institution Agreements

HEP ASICs have evolved to require high channel counts and broad functionality approaching Systems on a Chip SoC complexity.

- **Require coordinated effort of a broad range of Experts. Resulting in the need for a large multi-institutional team. This worked for RD53b BUT**
- **There is currently NO similar model for this kind of design team in the US.**
- **Collaboration on designs is a non starter if our NDA agreements don't allow sharing as with the CERN "frame contract"**

- **IMEC was chosen by CERN to negotiate the successful TSMC 65nm multi-institutional contract and *we learned recently* IMEC would consider pursuing a similar agreement with US institutions.**

→ We need to Prioritize finding and supporting a third party intermediary (like IMEC) to negotiate a multi-institutional contract between US institutions and and one or more diverse foundries like TSMC.

Important Technical Development to Enable Breakthrough Innovation

- **Enabling NEW ASIC Functionalities of Common Interest**
- **Areas of Interest for Priority Support for potential Breakthrough**

Important Technical Developments

Reduced Radiation Sensitivity Techniques and Technology

Extreme Track Density and high collision rates for inner detector trackers already lead to total dose radiation level requirements above 500MRad. Radiation requirements will grow as higher energy high luminosity machines are developed for future colliders.

- **A near term PRD to explore total ionizing dose, bulk damage, SEE and SEU sensitivities in 28nm technology could be helpful in finding a suitable technology to replace the 65nm technology presently used in these detectors and eliminate a need for further replacement of these trackers for the duration of the HL-LHC runs.**
- **A PRD for future developments will be to develop a better understanding and improved predictability of the radiation tolerance of HEP accessible ASIC technologies.**

Important Technical Developments

On-Detector Processing for Low-Power, High-Performance Sensor Readout

Significant gains in data reduction are possible utilizing reconfigurable logic as witnessed by the high growth of FPGA processing.

- **Implementing open source RISC-V processors in next Generation ASICs**
  - **Allows reconfigurable processing using C code instead of Verilog code. More familiar to the physics community.**
  - **Likely result is more abstracted information from the front end**
  - **Large savings per channel in power and off detector bandwidth.**

RISC-V

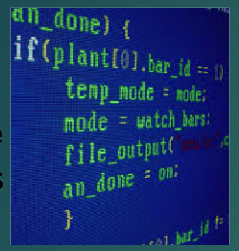
- RISC-V is an open-source instruction set architecture (ISA) developed at UCB
- The ISA is the logical definition of a microprocessor that allows software development (interface between hardware and software)
- Prior to RISC-V, a license to ARM or similar ($$) would be needed for System-on-Chip (SoC) development
  - Since ARM is proprietary, no custom instructions allowed (unless you paid ARM)
- Since RISC-V is open-source it is royalty- and license-free and it is possible to extend it
  - RISC-V makes it practical to take advantage of custom computing

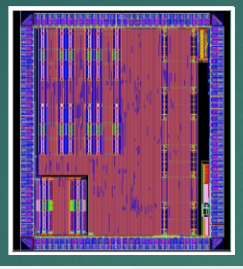
Matching Machine to Algorithm

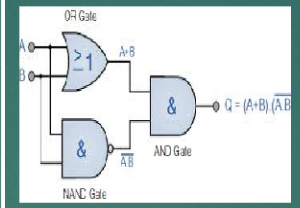
Application-Specific Computing

Code → Convert to → Hardware

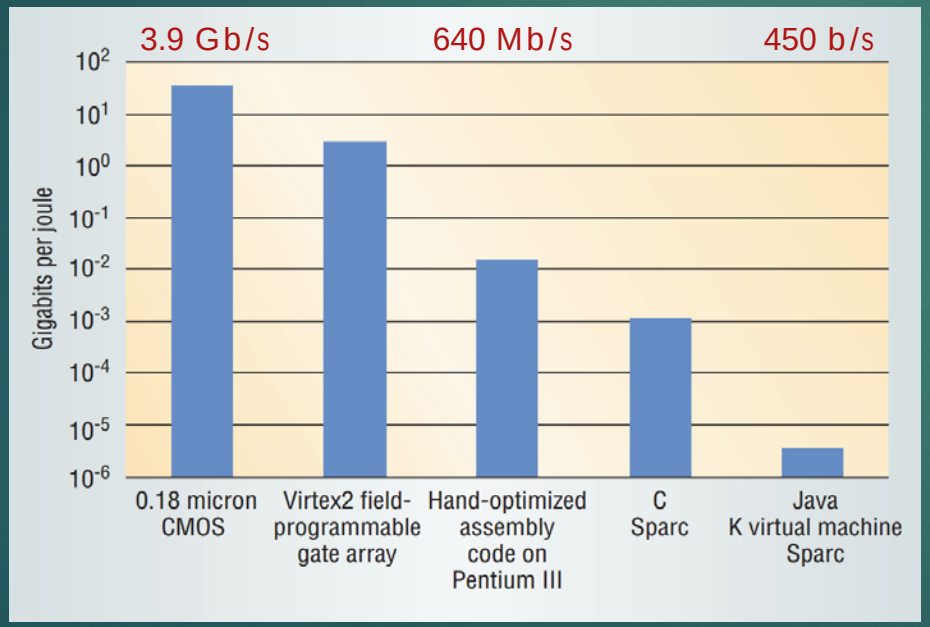
DFT & Climate Kernels







One powerful method in matching machine to algorithm is to convert the core code for an algorithm into custom hardware



128-bit key AES encryption algorithm

Schaumont et al., *IEEE Computer*, 3/2003

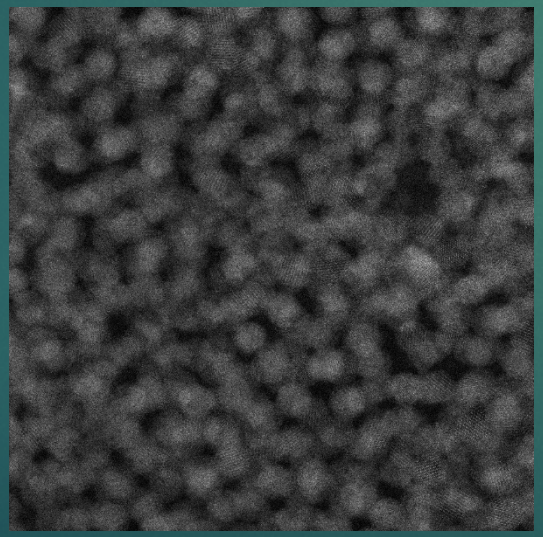
- Over 6 orders-of-magnitude difference in performance (or equivalently, efficiency at fixed performance) by moving towards increasingly specific hardware
- Custom instructions can provide good balance between flexibility and efficiency

Custom Instruction : FFTAccel

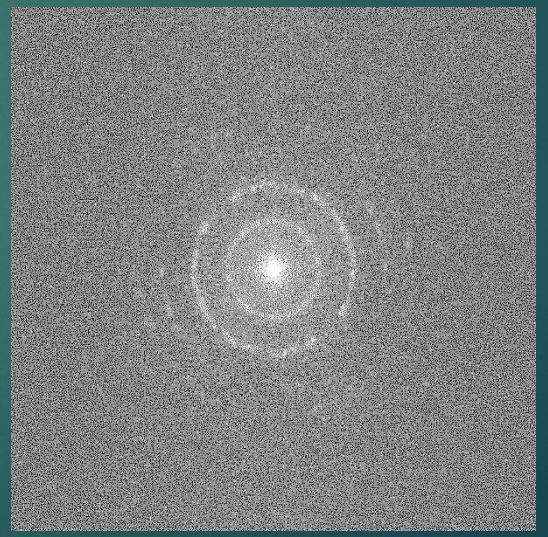
- Analyzing the FFT Accelerator with a 2-D FFT (using powder diffraction experimental data)

- FFT Accelerator runs around 100x faster than single-threaded CPU
  - SciPy FFT on Intel Core i7-5930K @ 3.50GHz: **~265ms**
  - FFTAccel (Floating): **~2.10ms** FPGA.. an **ASIC** implementation could be 10X faster...

Original Image



FFT



Important Technical Development

AI and Neuromorphic and Asynchronous Readout Techniques:

Machine Learning (ML) and Artificial Intelligence (AI) systems are changing the way large data sets are interpreted increasing the potential for discovery of current experiments.

- **Expect these techniques to have more powerful impact when implemented in-situ or on hardware optimally designed to implement neural networks.**

  Implementations

  - **Study Machine Learning architectures for HEP problems**
  - **Improve ability to pull abstracted data from HEP detectors**
  - **Study potential for on detector *multi-channel* synthesis of event parameters.**

Important Technical Development

Power Management and Conditioning:

CMOS Technology advances have towards very high gate count and lower supply voltage operation. Resulting in growing complexity that needs to be supplied by higher current and Lower voltage devices.

- **Traditional cabling treatments result in larger diameter (therefore more inert mass) supply cabling and higher sensitivity to resistance between the supply & load.**
- **Low Voltage results in circuits with higher sensitivity to supply noise**

- **Recently ASICs have included Low Drop Out Linear Regulators on chip.**
- **Next generation ASICs will want to follow the commercial industry examples and add DCDC converters on chip.**
- **PRD - These commonly applicable blocks can be developed independently and implemented following journal article design examples or directly by borrowing IP. An FOA topic could be helpful to find development interest.**

Important Technical Development

- **Wireless Communications:**

  Near term benefit: Free up high speed physics data channels from detector status and control information:

  - **First implementations:**
    - **Slow Control operational modes, power sequencing, set and readback control registers, code revision and checking of future detector systems**
    - **Environmental Monitoring Voltages, Currents, Temperatures**
  - **Future:**
    - **Triggering**
    - **Regional Data**
    - **???**

Important Technical Developments

- **High speed Data transmission interfaces:**
- **PRD <u>Improvent of Copper links and encoding techniques</u>**
  - **Phase II Pixel track detectors will last only a few years at HL-LHC before requiring replacement due to the extreme radiation environment.**
  - **In the intervening time we can likely improve the bandwidth of data by a factor of 5 or 10X utilizing commercial techniques such as PAM4.**
- **PRD <u>Optical Transmission-</u>**
  - **There is a large transfer BW gap between our HEP specialized 10Gb links and industrial capabilities now reaching 400Gbps.**
  - **Environmental constraints limit our ability to just upgrade our links**
    - **Radiation Sensitivity, Mass and Power for TX/RX, cold temperatures**
    - **We need to look to industry for improved techniques and implement these in our communities.**

Important Technical Development

Cold Electronics for Liquid Noble detector systems:

- **Technology Choices for operation at (-100 to 250C)**

  Commercial foundries cover models/reliability down to -40C

PRD –

- **Technology Characterization including lifetime at Cold Temperatures**
- **Development & Characterization of custom digital library cells for reliable decadal operation.**

Important Technical Development

- **Cryogenic Applications 4K and below:**
- **Investigate Technologies, Model parameters**
- **HEP applications of interest**
  - **TES**
  - **MKIDs**
  - **Bolometers for Cosmic Microwave Backgrounds..**
  - **Applications in QIS Quantum Interference Science**

Important Technical Development

- **Picosecond High precision timing:**
  - **Front End Specialization dependent on Sensor Technology**
  - **Low power High Speed Demands High Speed Technologies such as**
    - **High Intensity Hadron Machines with 100 MRAD & higher lifetime requirements**
      - **Small Feature size CMOS 65, 28nm and possibly smaller**
    - **Electron Machines, Cold Detector Noble Liquid Detectors with Photon readout**
      - **Small Geometry CMOS possibly combined with Silicon Germanium front ends.**

Important Technical Development

- **Standalone and 3D-integrated MAPS:**
- **MAPs are an enabling technology for tracking systems at future colliders.**
  - **Economical utilizing Commercial ASIC processes for sensor & readout.**
  - **Eliminates sensor – readout electronics interconnect issues.**
  - **Makes consideration of 500m^2 trackers plausible.**
- **PRD In order to maintain the US's historic leadership in tracking systems, a coherent US program of study is urgently needed in order to compete with existing European and Japanese programs.**

Summary

- The highest HEP ASIC Instrumentation priority is to support a healthy mix of Physicists and Engineers in the readout design teams
  - Maintain Expertise in the field by having interim projects to train others and develop readout techniques suitable for future HEP detectors
- We need to examine available design and fabrication support for HEP groups
- To pursue multi-institutional design agreements with ASIC manufacturers
- Provide training opportunities that encourage young people to join ASIC design teams

We need to support work in future detector related technologies

- Funding efforts to explore techniques and prepare blocks that we will need for our next generation detector systems.
- Develop detector specific understanding of unusual environmental issues created by extreme conditions related to temperature and radiation damage.