Chronopixel CMOS Sensor Development for the ILC

Jim Brau, *Nikolai Sinev, David Strom*
University of Oregon, Eugene, Oregon

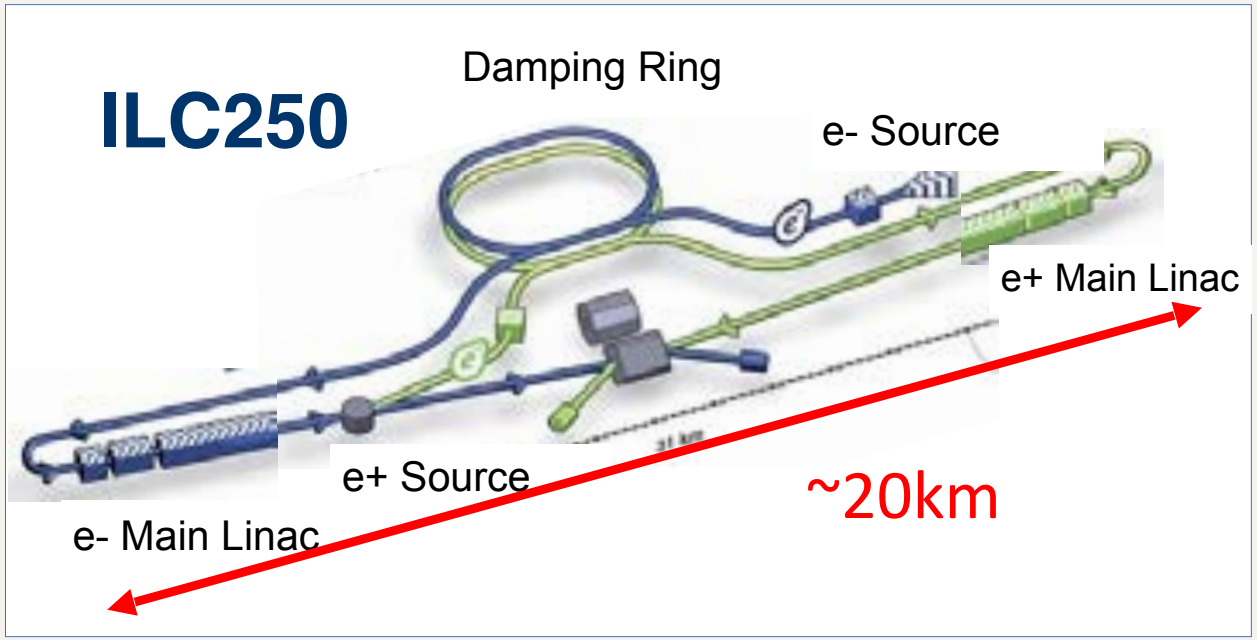
*Oliver Baker, Charles Baltay, Christian Weber**
Yale University, New Haven, Connecticut

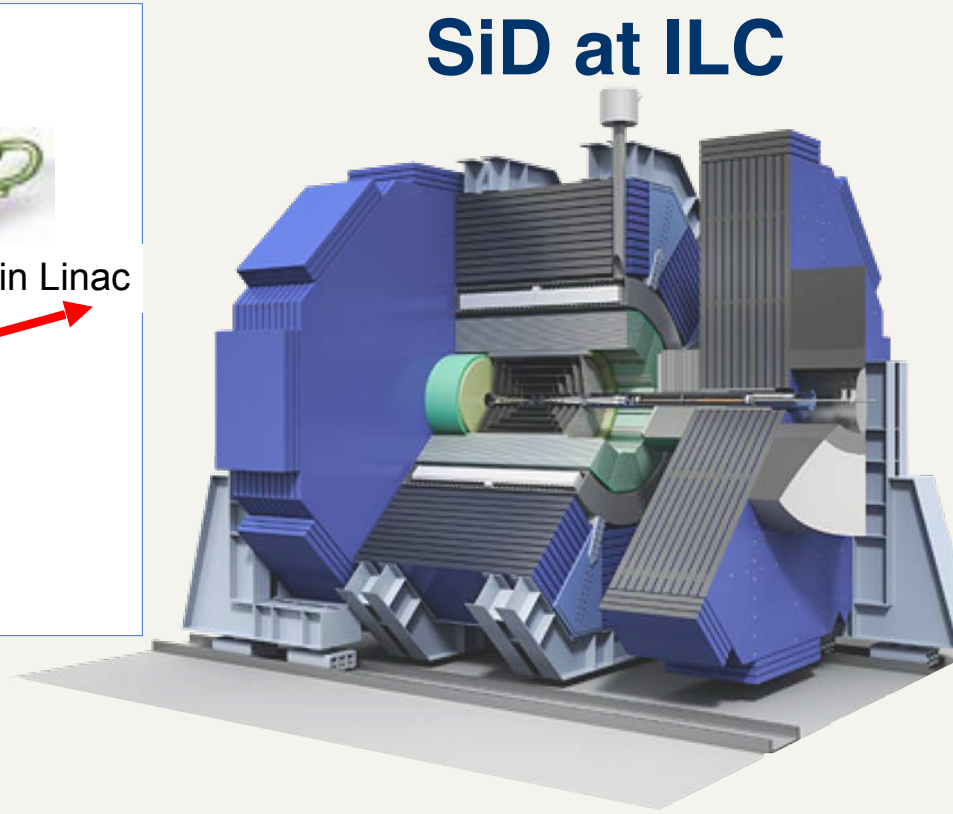
EE work has been contracted to Sarnoff Corporation/SRI

* current address: Brookhaven National Laboratory

Note: Many of these slides are based on originals prepared by Nikolai Sinev and Christian Weber

First stage - 250 GeV (Higgs Factory)
Ultimately higher energy: 0.5 - 1 TeV

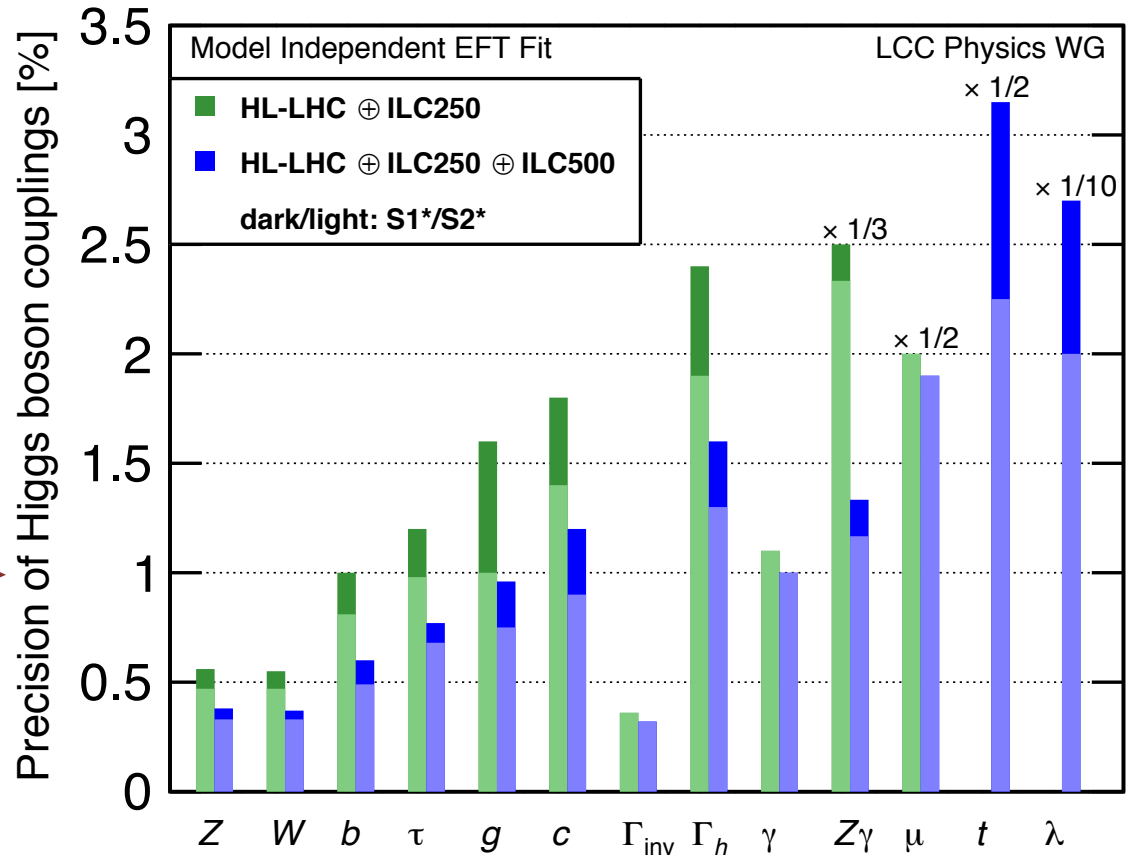




Higgs precision Higgs at the ILC

"Model-independent" EFT fit

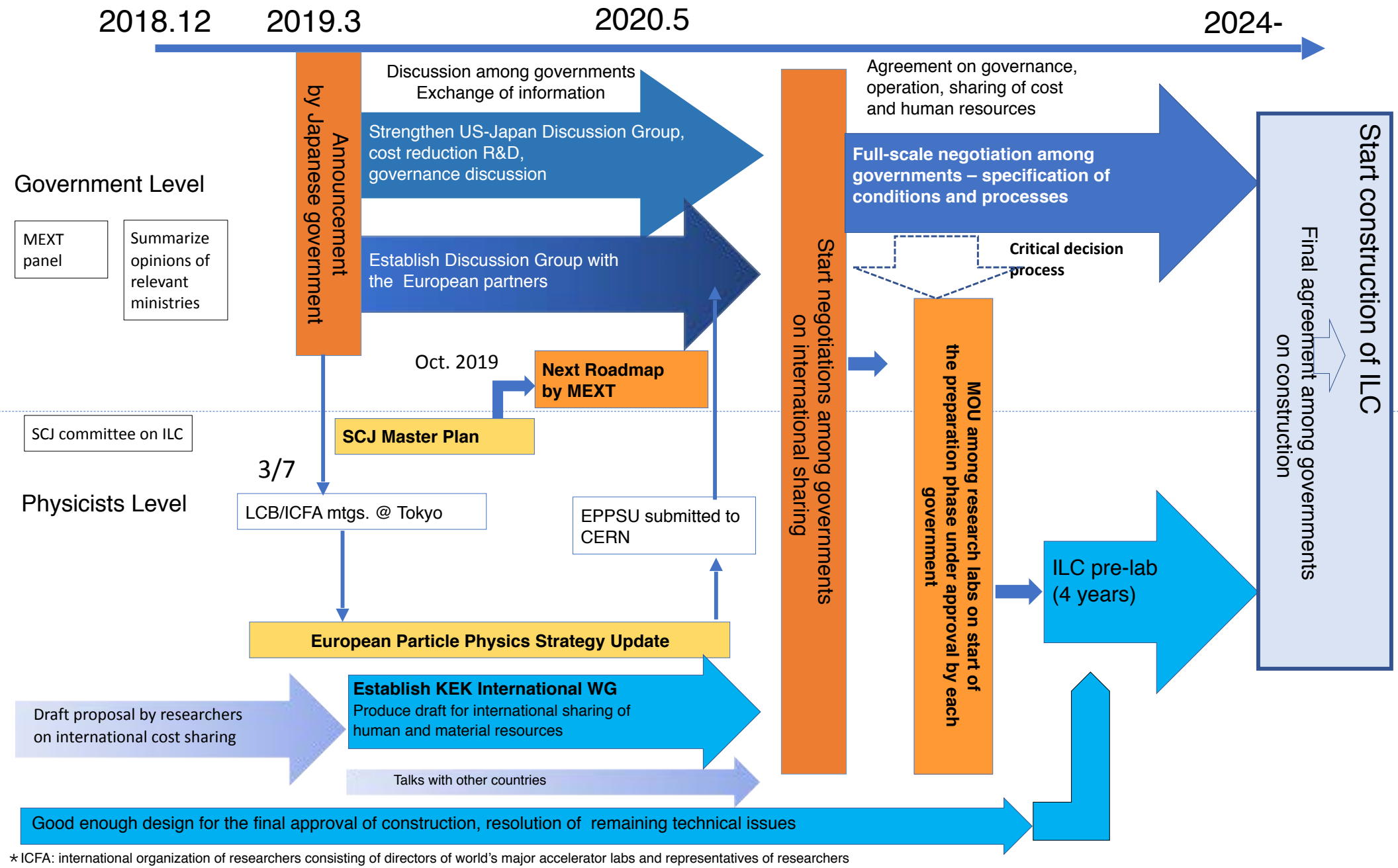
~1 % required to access New Physics beyond HL-LHC direct search



Highly **model-independent** analysis of EFT:
Phys Rev D97, 053003 (2018)

arXiv:1903.01629

Processes and Approximate Timelines Toward Realization of ILC (Physicists' view)

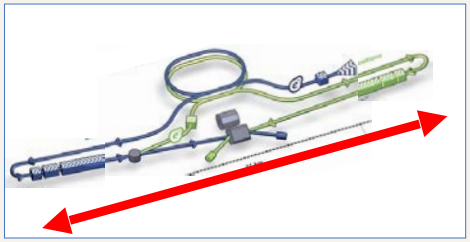


* ICFA: international organization of researchers consisting of directors of world's major accelerator labs and representatives of researchers
* ILC pre-lab: International research organization for the preparation of ILC based on agreements among world's major accelerator labs such as KEK, CERN, FNAL, DESY etc.

Status of ILC decision in Japan

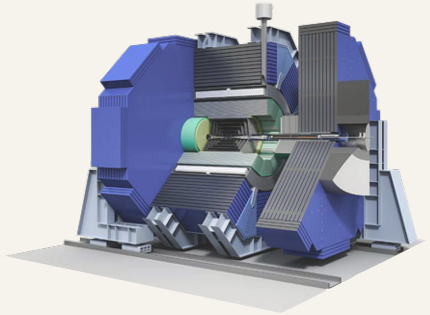
- Legislative branch (Diet) strongly supports hosting ILC in Japan.
- Two final national steps are needed to reach decision.
- **(1)** Science Council of Japan (SCJ) calls for proposals of large-scale research projects every three years, and recommends "priority programs" to MEXT. In the latest process in 2017, 20 programs were selected from 200 proposals.
- ILC will be evaluated for first time this year to provide evidence of support by broader Japanese academics.
- SCJ selected ILC for the reduced long list after 1/3 selection and invited ILC for an "interview."
- Results of final SCJ evaluation will be publicized officially in February 2020.
- **(2)** Next step will be MEXT Roadmap in 2020. Previous 2017 Master Plan/Roadmap process, MEXT made its own selection starting from the SCJ long list to create MEXT Roadmap.

ILC vertex detector requirements



ILC Beam environment:

Bunch crossing rate (Collisions rate) ~3 MHz
Number of bunches in bunch train up to ~3000
(first 250 GeV stage 1312)
Bunch trains interval – 200 ms. (5 Hertz)



Detector System

5 layers, ~2.4 cm - ~ 10 cm.
Length: ~20 cm with forward discs.
Pixel size < 15x15 μm^2 (space point resolution ~3.5μ).
Each pixel has 2x12 bit memory buffer to record 2 time stamps
during bunch train.
Room temperature operation with forced air cooling
and non-turbulent air flow.
Power dissipation for entire Vertex Detector to <~ 100 W.
Sparse readout allows full readout in 200 ms.
S/N ratio should be more than 30 (noise less than 25 e^-).

Chronopixel development history

2004 –First discussion with Sarnoff Corporation.

Oregon University, Yale University and Sarnoff Corporation collaboration formed.

2007-2010 - Prototype 1

5x5 mm chips, 80 each, containing 80x80 50 μm Chronopixels array

TSMC 0.18 μm ⇒ ~50 μm pixel

Epi-layer only 7 μm

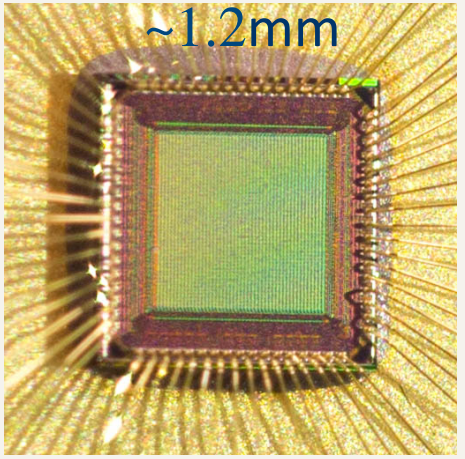
Low resistivity silicon (~10 ohm-cm)

2010-2013 - Prototype 2

MOSIS / TSMC. (48x48 array of 25 μm pixel, 90 nm process)

2014- Prototype 3

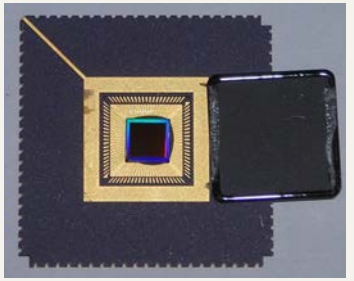
Chronopixel prototype 3

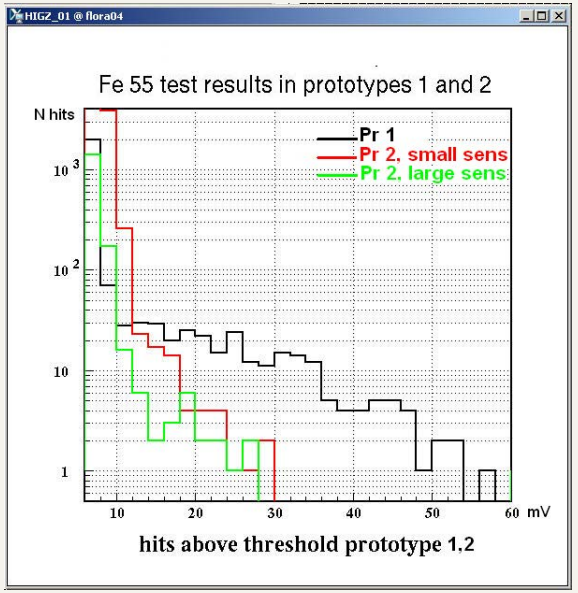


Summary of prototypes 1 and 2 tests

Prototype 1 demonstrated:

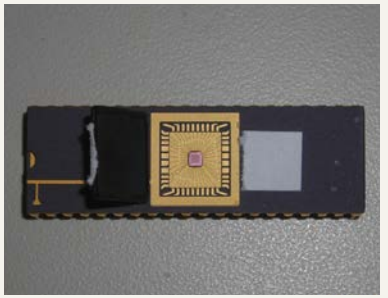
- Time stamp recording with 300 ns period (1 ILC bunch crossing interval)
- System to read all hit pixels during 200 ms interval between bunch trains (by implementing sparse readout)
- Pulsed power (2 ms ON and ~200 ms OFF) with preserved comparator performance.
- Noise figure achieved as 24 electrons rms, compared to spec of 25.
- Comparator offset spread a few times larger than anticipated.



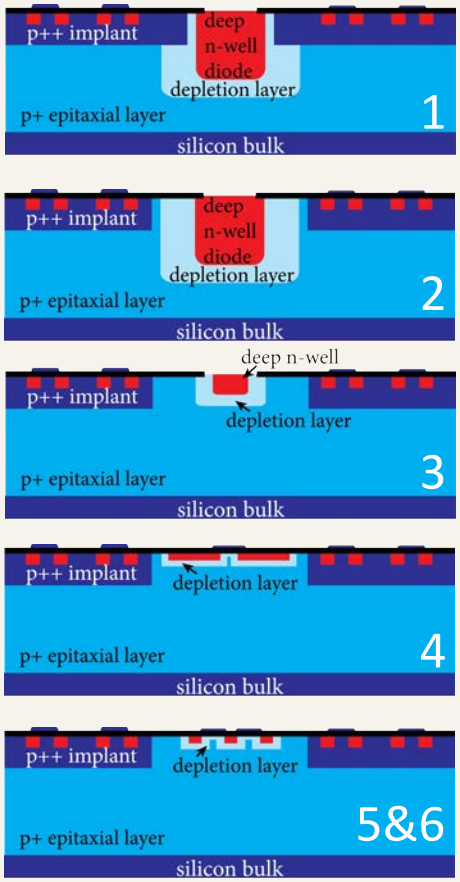


Prototype 2 demonstrated:

- All NMOS electronics without unacceptable power consumption
  - (not clear all NMOS electronics is a good alternative to deep P-well option)
- Comparators offset calibration with virtually any required precision using analog calibration circuit.
- Smaller feature size creates issues: sensor capacitance limits signal/noise ratio, stemming from 90 nm process design rules.



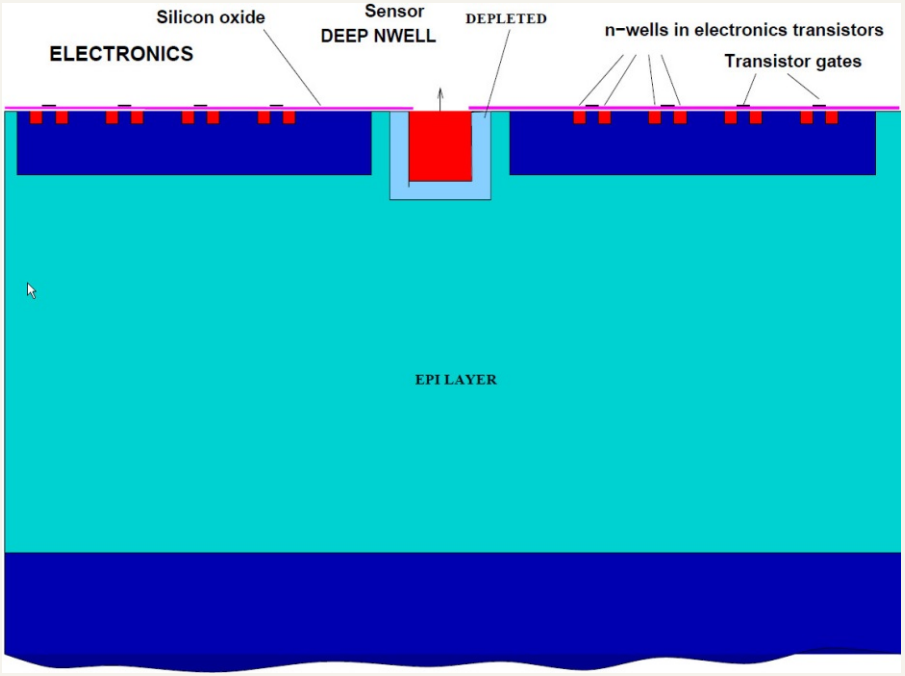
Prototype 3 - six sensor alternatives

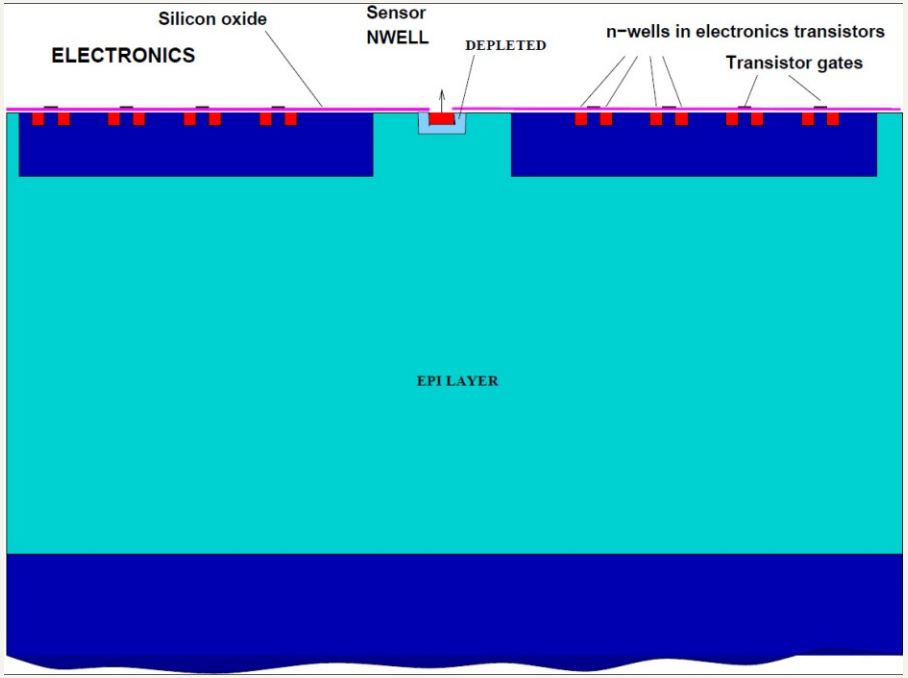


Six different sensor options were implemented on the same chip – 8 columns for each option:

1. Same as prototype 2 – for comparison.
2. Deep NWELL diode in the window in P++ layer - design rules waiver.
3. Shallow NWELL diode, also in the window - design rules waiver.
4. "Natural transistor" in the P++ layer window
   transistor is formed directly on P+ epi layer
   large source and drain diffusion areas
   gate connected to both source and drain and form sensor output.
5. Also "Natural transistor" but with 2 fingers
   source and drain are narrow
   gate also connected to both, as in option 4.
6. Same as 5, however gate is not connected to source and drain, but connected to external bias voltage.

Deep NWELL (option 2) vs. shallow NWELL(option 3)





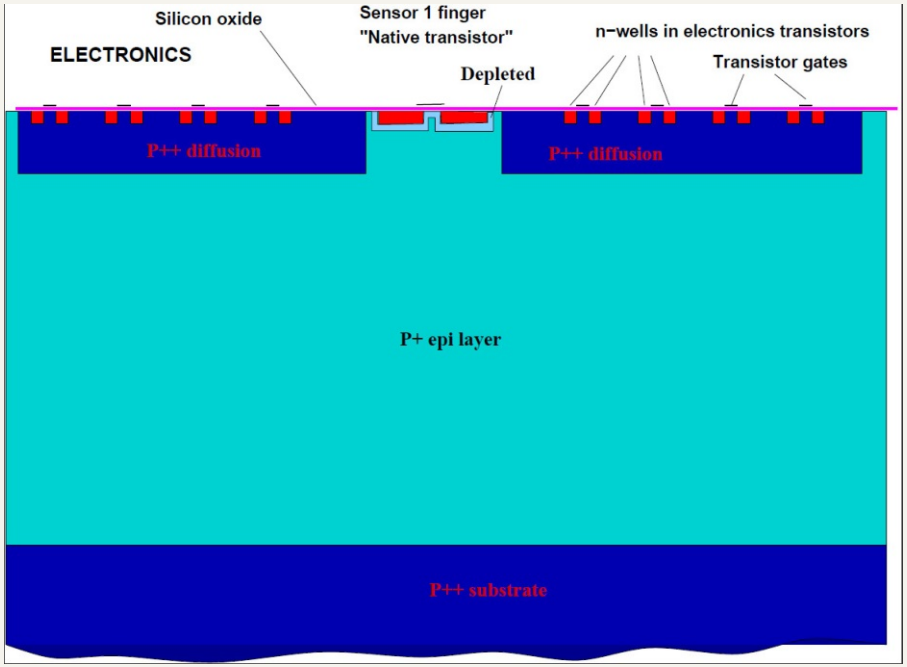
Deep NWELL (option 2)

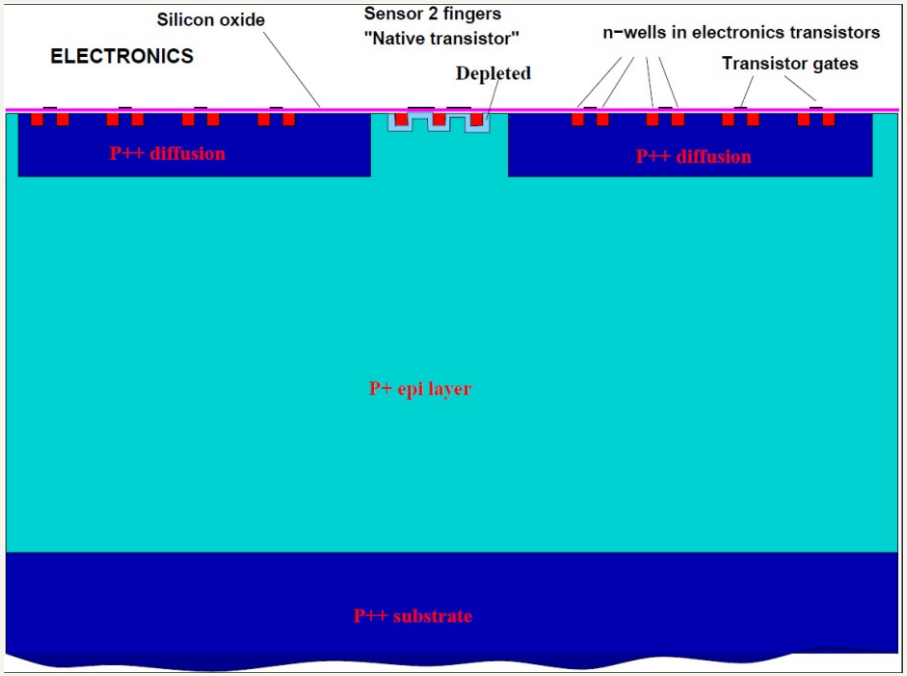
larger area and larger charge collection efficiency, but larger capacitance.

Shallow NWELL (option 3)

smaller area, but P++ acts as charge reflector. Window size may define charge collection efficiency.

Options with "Natural transistor"





Option 4 (1 finger)

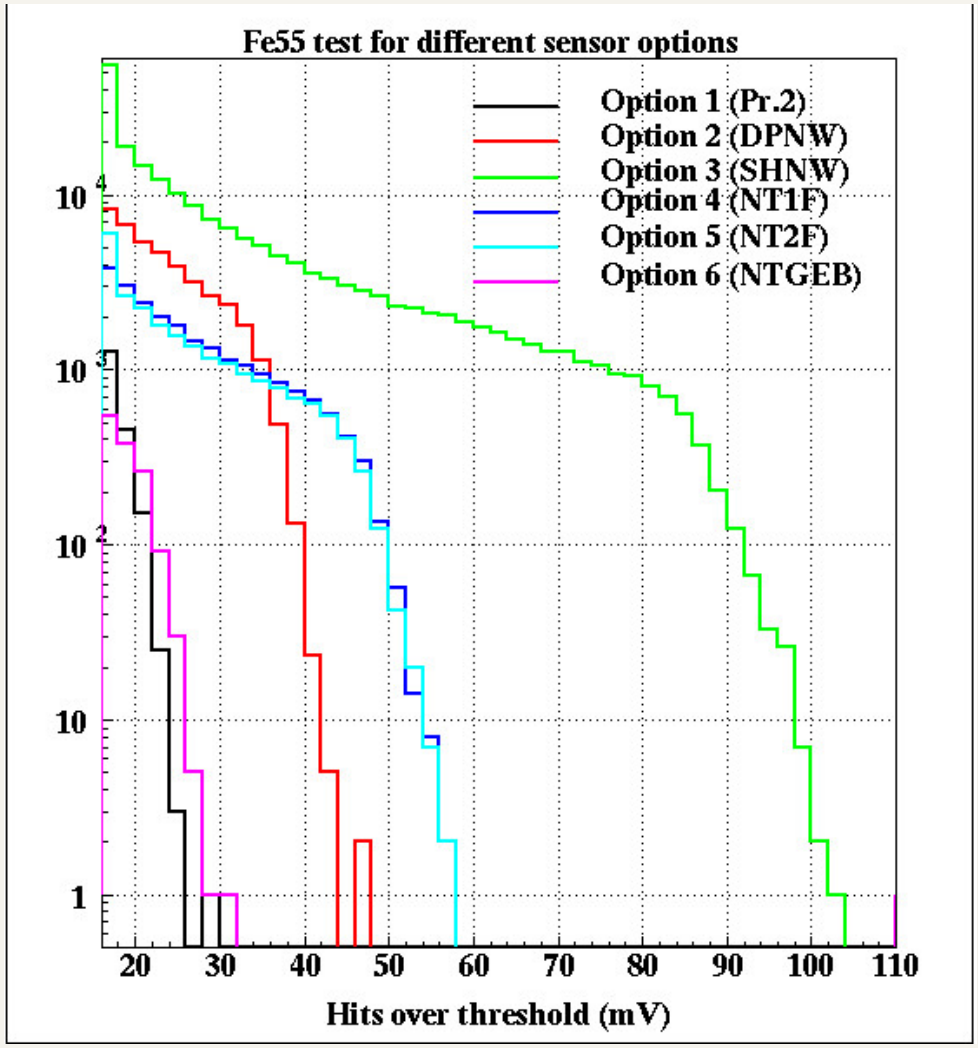
Larger nwells forming source and drain. Is charge collection efficiency better? What is impact of size on sensor capacitance?

Option 5 (2 finger, gate to source and gain)

Option 6 (2 finger, gate to external bias)

How do these two options behave ?

Fe55 sensor capacitance test

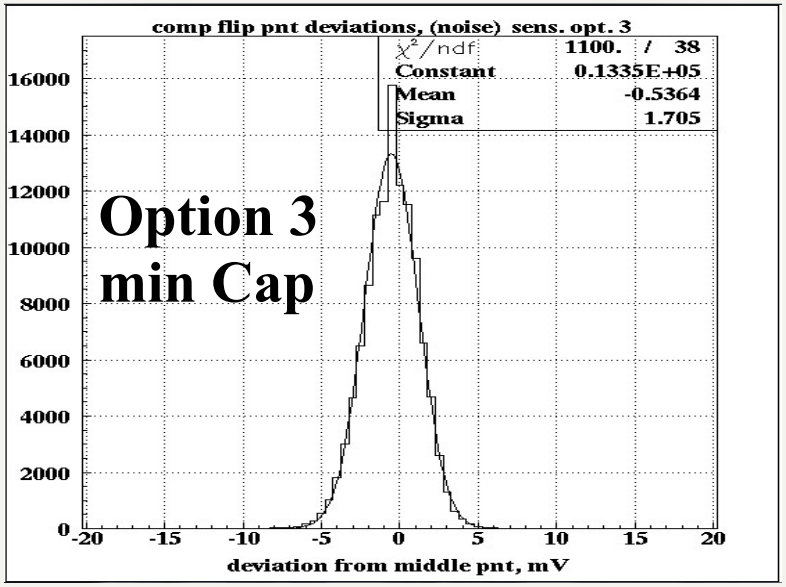


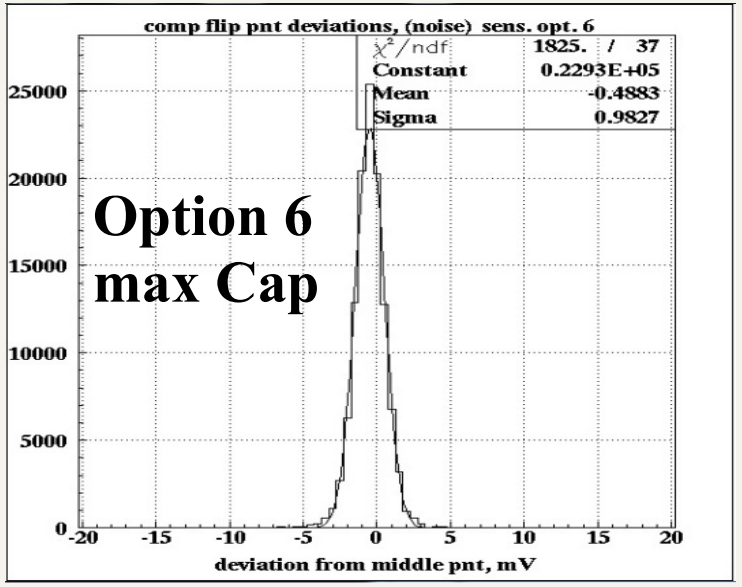
$$C = \frac{E_{\mathrm{Fe55}} \dfrac{1.6 \cdot 10^{-19} C}{3.6\ eV}}{V_{\max}}$$

$$E_{\mathrm{Fe55}} = 5.9\ keV$$

diode option	Capacitance (fF)	µV/e
1	9.0	18
2	6.2	26
3	2.7	59
4	4.9	33
5	4.9	33
6	8.9	18

Sensor noise measurements





Option #	Noise r.m.s (mV)	Noise r.m.s (# electrons)
1	1.12	63
2	1.08	42
3	1.7	29
4	1.21	37
5	1.23	38
6	0.98	54

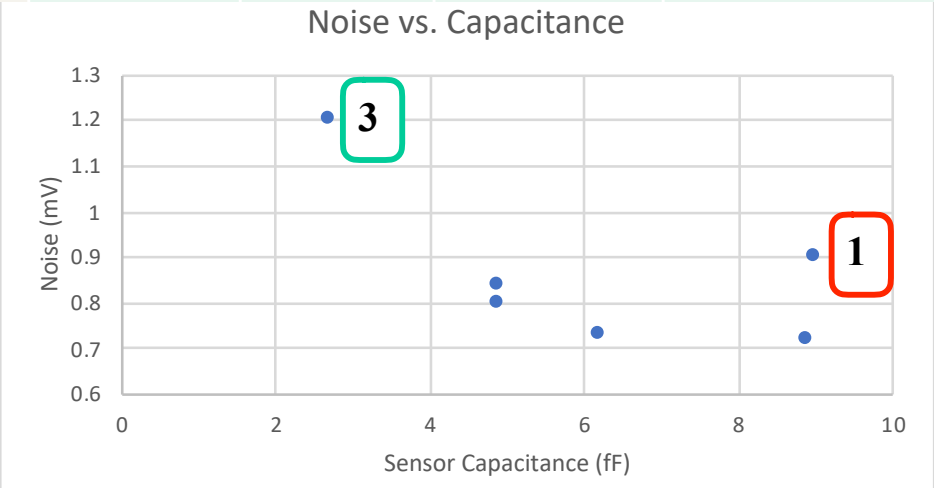
Noise larger, than expected from kTC noise formula. Additional noise pick up.

Noise observed vs expected

Option	sigma obs. (mV)	sigma exp. (mV)	Sqrt ($\delta^2_{ob} - \delta^2_{ex}$) (mV)
1	1.12	0.67	0.9
2	1.08	0.8	0.73
3	1.7	1.21	1.2
4	1.21	0.9	0.8
5	1.23	0.9	0.84
6	0.98	0.67	0.72

Anomalous extra noise, near pulse control

Max extra noise, min cap



Extra noise pick up appears to occur mainly through capacitive coupling to the sensor

Chronopixel prototype 3 discussion

Best performance from option 3

shallow NWELL,

small capacitance, large signal,

violates design rules

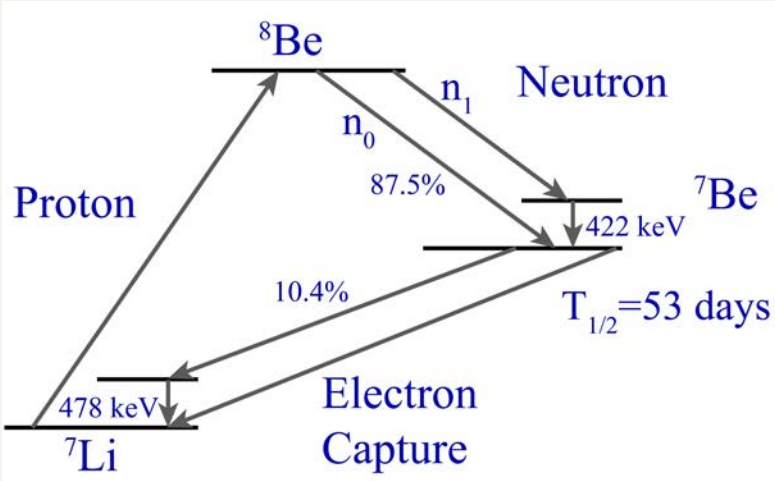
However, option 3 sensor area is only 2.74 μm^2,

while options 4 and 5 – natural transistors – have sensor (n+ diffusion area) 19.36 μm^2 , important for charge collection.

Also, p++ implant reflects charge - competes with sensor size.

Future studies needed to investigate the relevance of the competing features to produce optimal design.

Neutron Irradiation Test



G.H.R Kegel et al, IEEE TNS vol39, No6 (1992)

- 4 MeV proton incident on ^{7}Li target to produce neutrons
- Proton beam current and neutron rate monitored during irradiation test
- Total number of neutrons created is eventually determined by radiation assay of target
- Chronopixel works after 10^{13} n_{eq}/cm^2

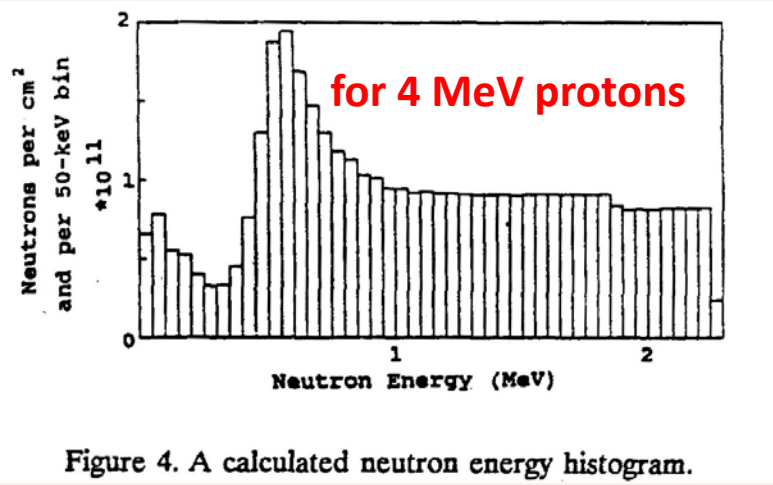
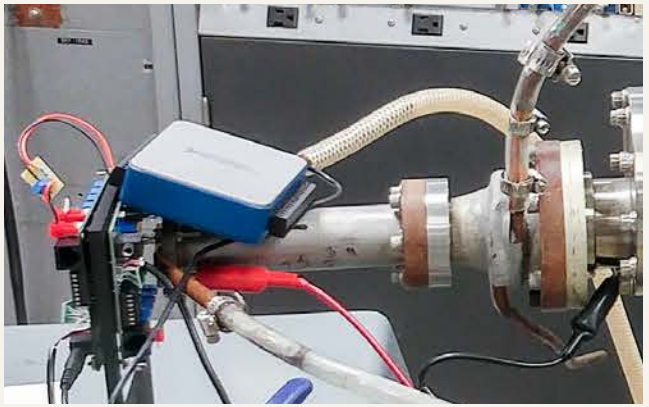


Figure 4. A calculated neutron energy histogram.



Lithium target

Total integrated dose test

Test resistance w.r.t. total ionizing dose received

1MeV protons

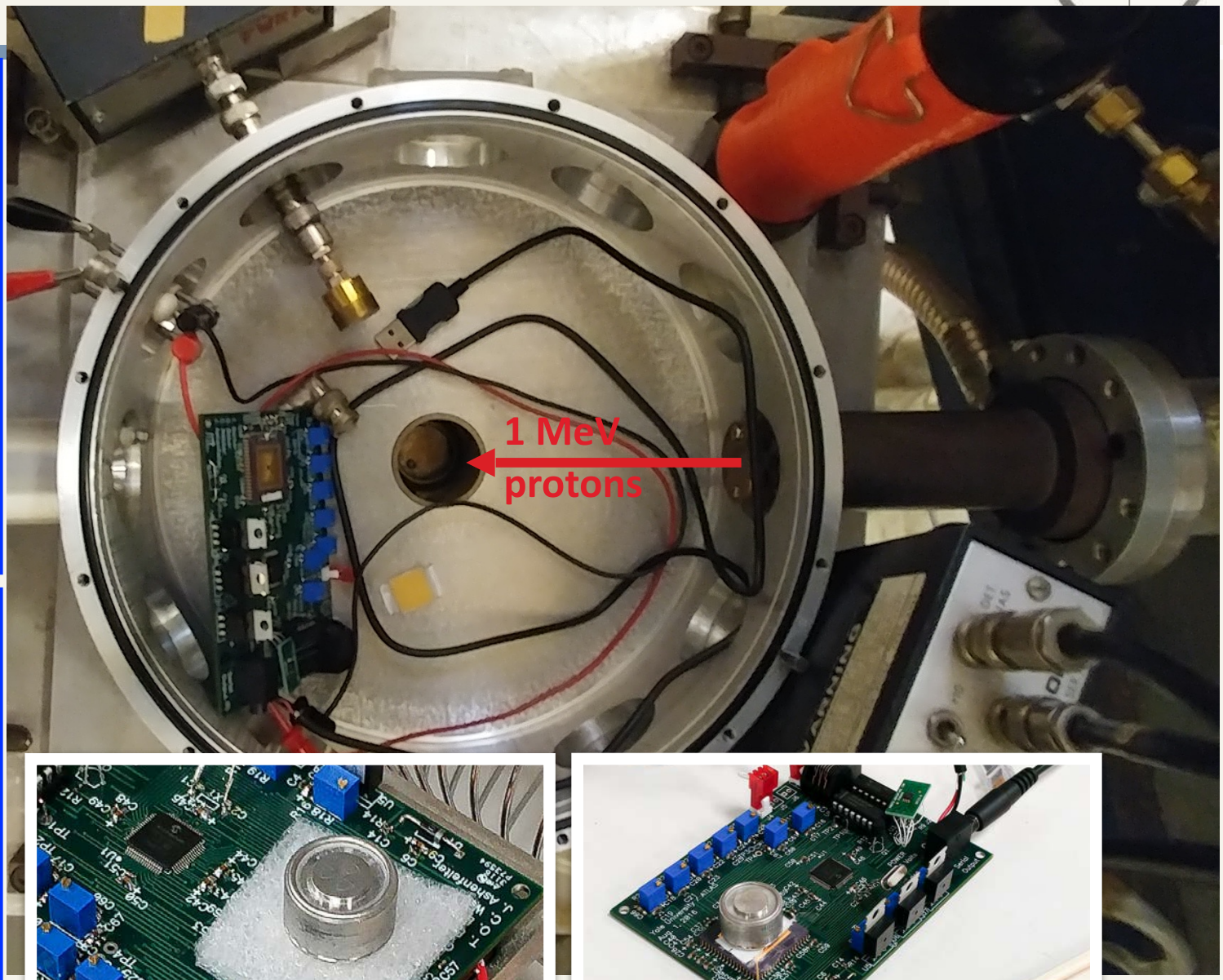
4 nA current
(large dose rate!)

Energy deposited within first 8 μm of silicon
(≈ epi layer)

After each irradiation run

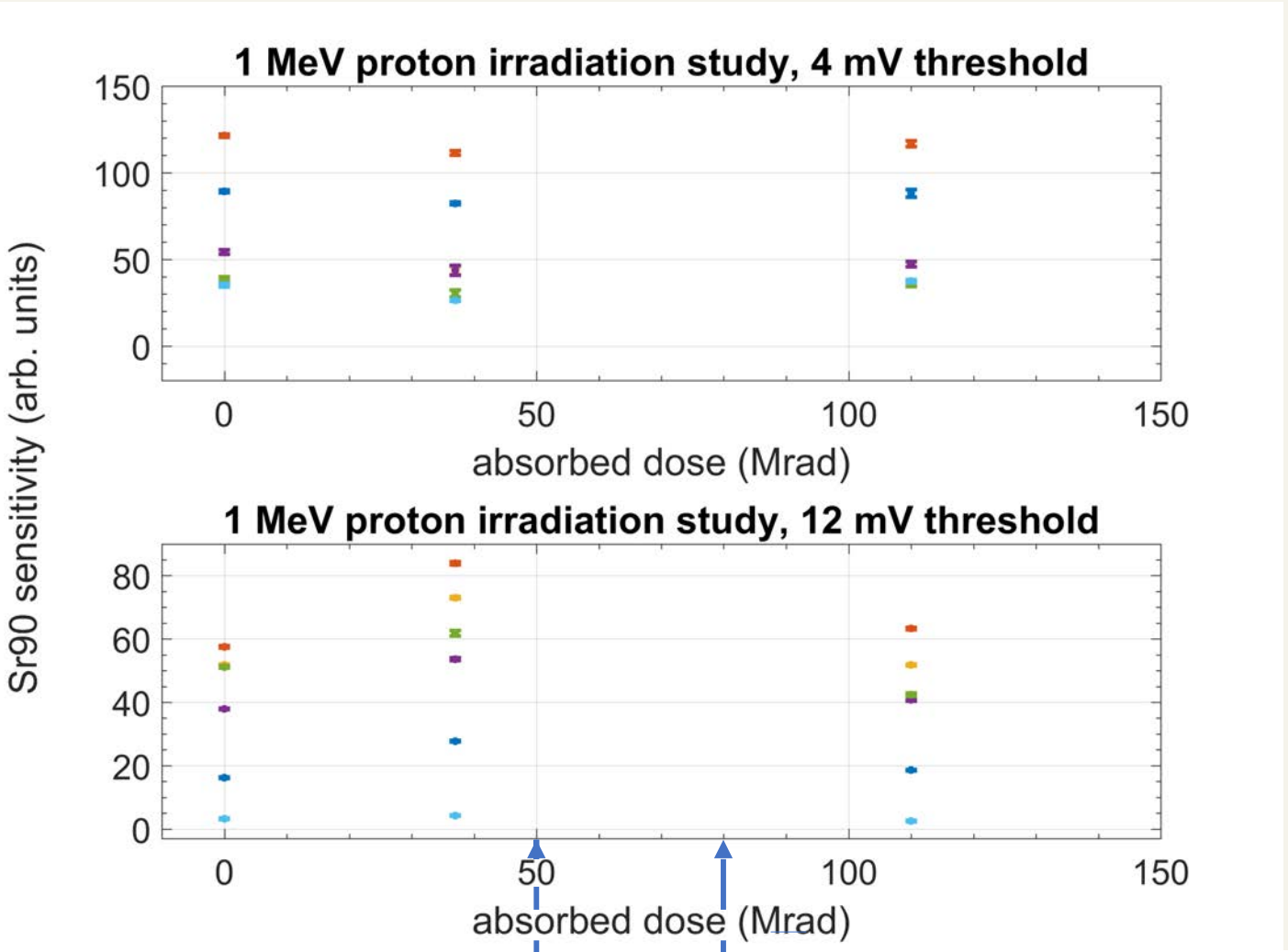
Anneal at 60°C for 80 min

Test for change in count rate using Sr-90 source
($t_{1/2} = 29$ yrs, 2.3 MeV β, minimum ionizing)



MeV proton irradiation results

- sensor type 1
- sensor type 2
- sensor type 3
- sensor type 4
- sensor type 5
- sensor type 6



ATLAS phase 2 pixel detector, outer layer

ATLAS phase 1 pixel detector, inner layer

ILC Chronopixel performance

Parameter	ILC Requirement	Prototype Tests
Detector Sensitivity	10 µV/electron	59 µV/electron
Detector Noise	25 electrons	29 electrons
Comparator Accuracy	0.2 mV RMS	0.2 mV RMS
Sensor Capacitance	10 fF	2.7 fF
Clocking Speed	3.3 MHz	7.3 MHz
Charge collection time	300 nsec	20 nsec
Readout Rate	25 Mbits/sec	25 Mbits/sec
Power Consumption	0.13 mW/mm^2	OK by estimate
Radiation Hardness	10^{11} neutrons/cm^2/yr	10^{13}neutrons/cm^2 or 110 Mrad

Conclusions

Following a multi-year R&D effort, Chronopixel prototype 3 demonstrated a working ILC CMOS vertex sensor that satisfies the ILC design requirements.

Radiation exposures have shown the performance is maintained for ILC exposure levels.

Future development will further improve and refine the details:

- **Refine analysis of option trade-offs.**
- **Thicken epi layer and increase resistivity.**
- **Expand detector area.**
- **Reduce small cross talk issues.**
- **Perform tests with minimum ionizing particles.**
- **Demonstrate min-ion efficiencies.**

We gratefully acknowledge support by the Department of Energy, Office of High Energy Physics