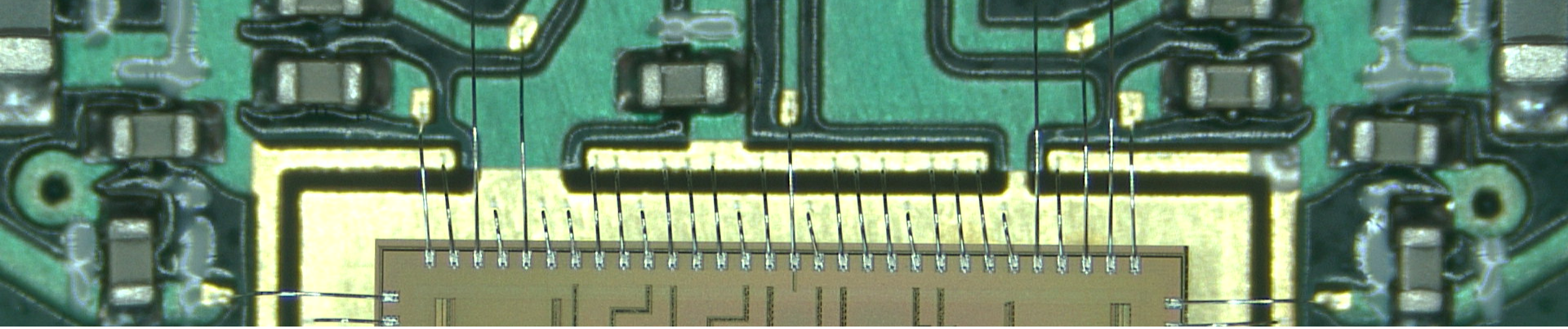
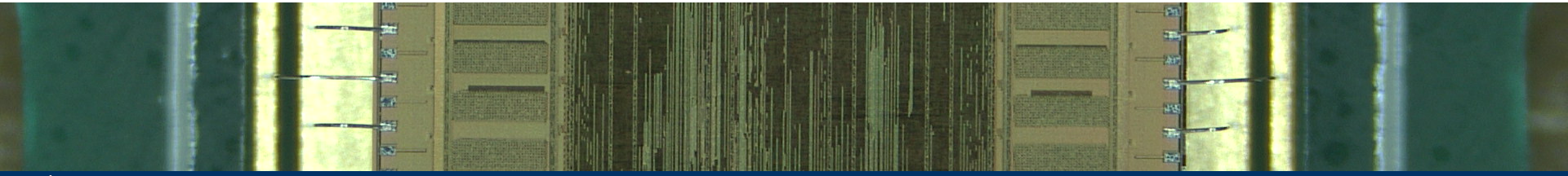


Pixelated LArTPC R&D: LArPix

Peter Madigan

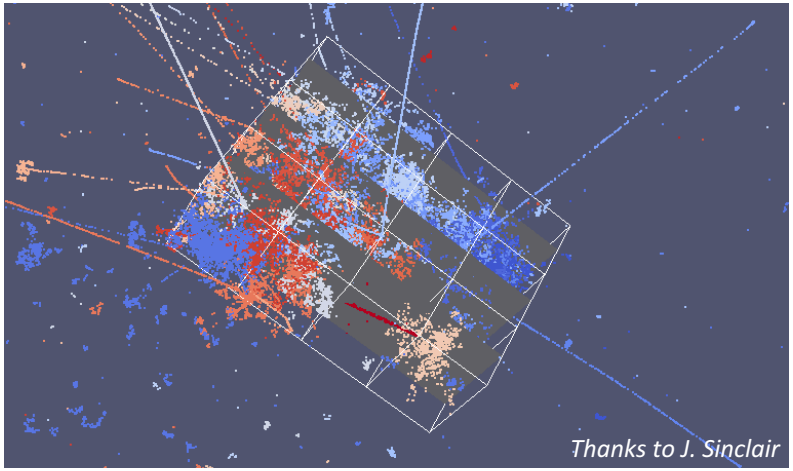
UC Berkeley / LBNL

CPAD 2019

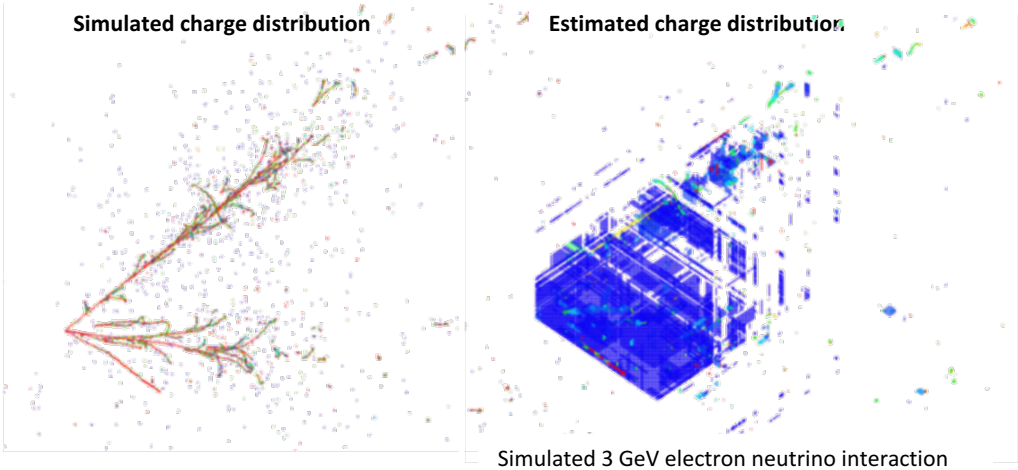


Pixelated LArTPCs

Simulation of a single neutrino beam spill at the DUNE near detector, colored by neutrino interaction.



Wire readout leads to reconstruction ambiguities:



Simulated 3 GeV electron neutrino interaction

For DUNE

- Near detector is expected to have many neutrino interactions per beam spill
- Drift time >> spill -> *substantial neutrino pileup*
- Ionization is sparse -> *overlap is small in 3D*

Reconstruction needs access to full 3D information!

Pixelated TPCs as the answer:

Demonstration of pixelated anode plane:

- Univ. of Bern / ArgonCube

Test beam demonstration of pixelated LArTPCs:

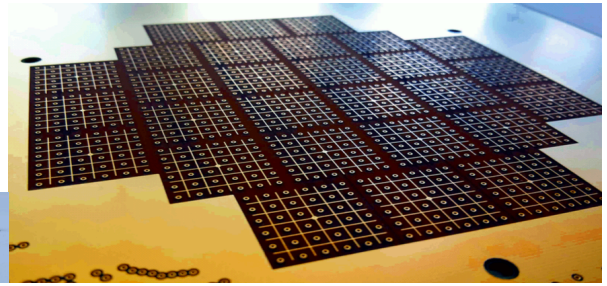
- PixLAr in LArIAT at Fermilab *(JINST 13 C02008)*

Demonstration of 3D LArTPC readout (LArPix):

- LArPix at LBNL and Univ. of Bern *(JINST 13 P10007)*

ArgonCube

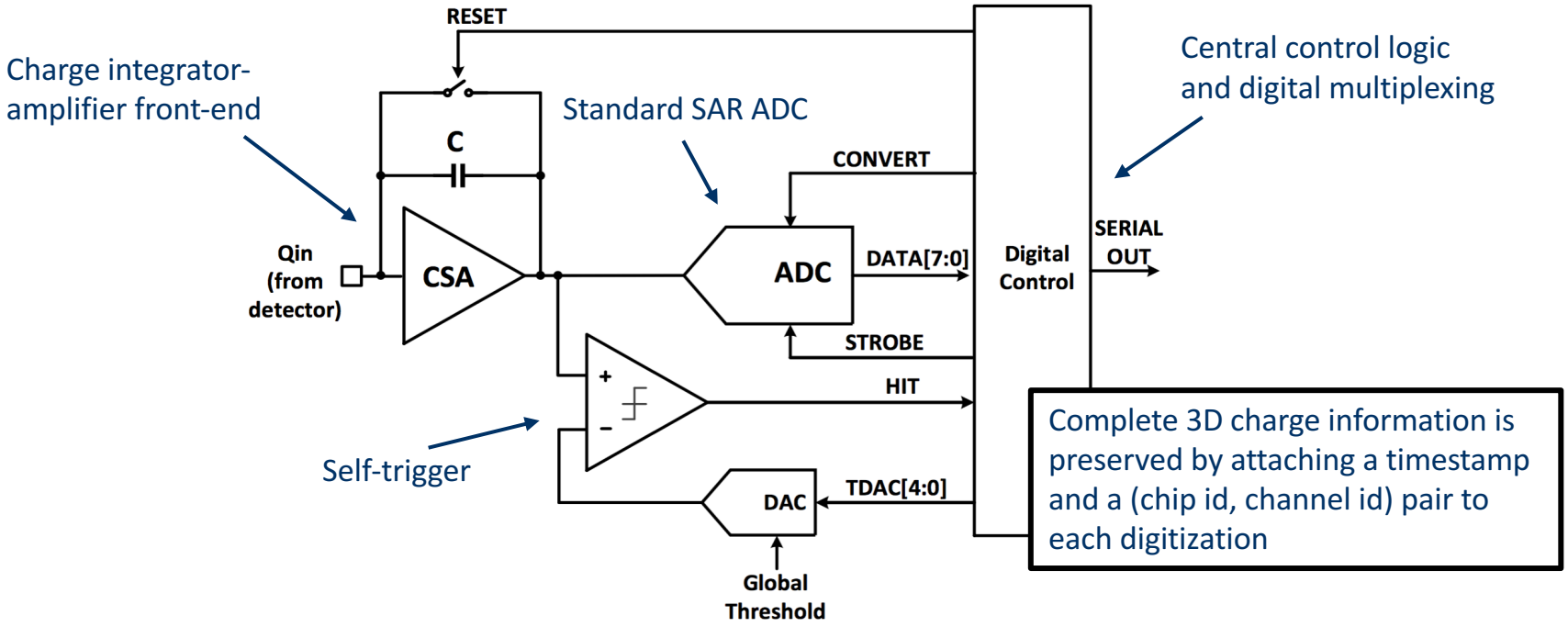
P X L A R



A prototype LArTPC pixel sensor (University of Bern)

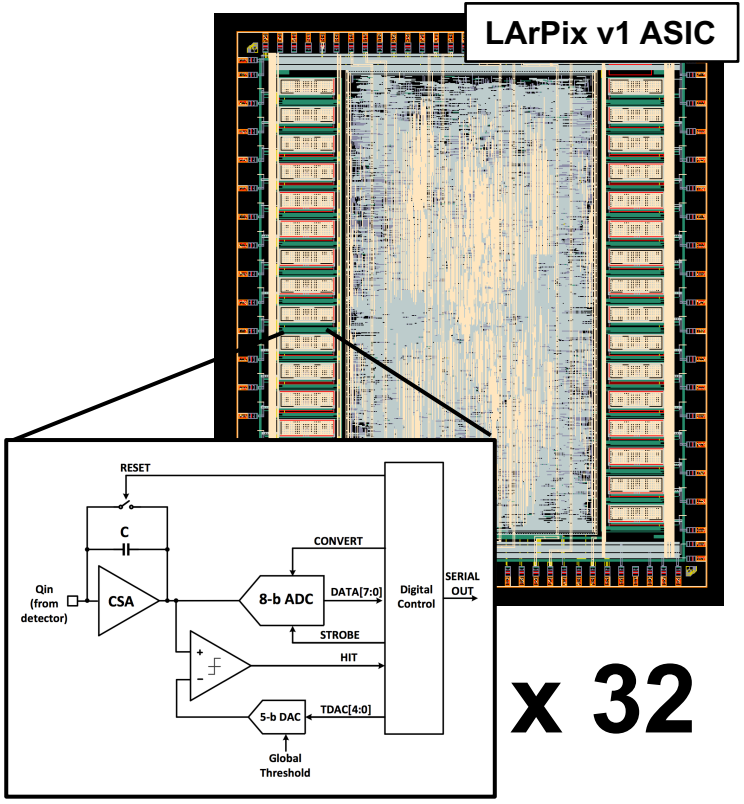
LArPix concept

The challenge - Develop a cold IC that uses very little power and provides full 3D charge information



The idea - Use a self-triggered ADC for each channel to limit chip activity and thus power consumption

LArPix concept demonstration



LArPix-v1: Cryogenic-compatible 180 nm CMOS ASIC

- Designed by LBNL IC design group in 2017

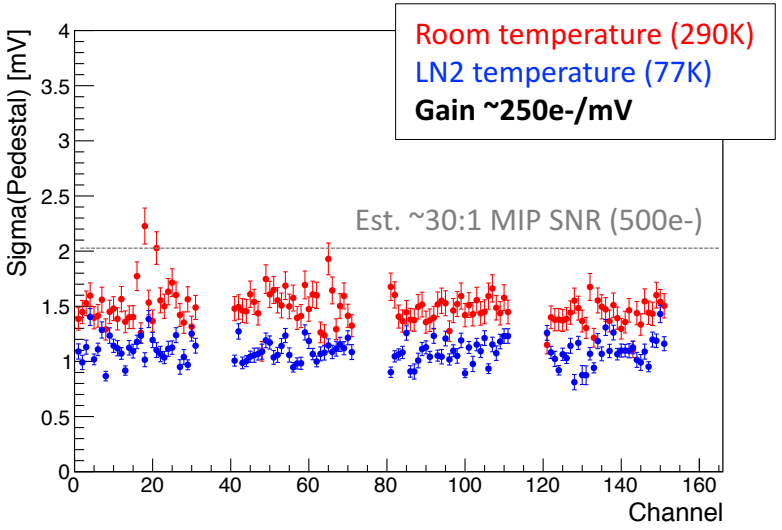
Provides 32 channels / chip with:

- Charge integrator / amplifier
- Self-trigger
- 6-bit ADC

Wire-bonding to charge collection pads on PCB provides 3mm active area per channel

	Target	**290K**	**77K**
Power [uW/ch]	<~100	-	62
Noise [e- eq.]	<~1000	375	275
Leakage [e/ms]	<~1000	500	0.005

Meets all critical design targets!



Used successfully to read out complete 3D charge information of kg-scale LArTPCs!

See JINST 13 P10007 for more details…

Example LArPix events

See http://portal.nersc.gov/project/dune/larpix/ for an interactive event display of raw LArPix data

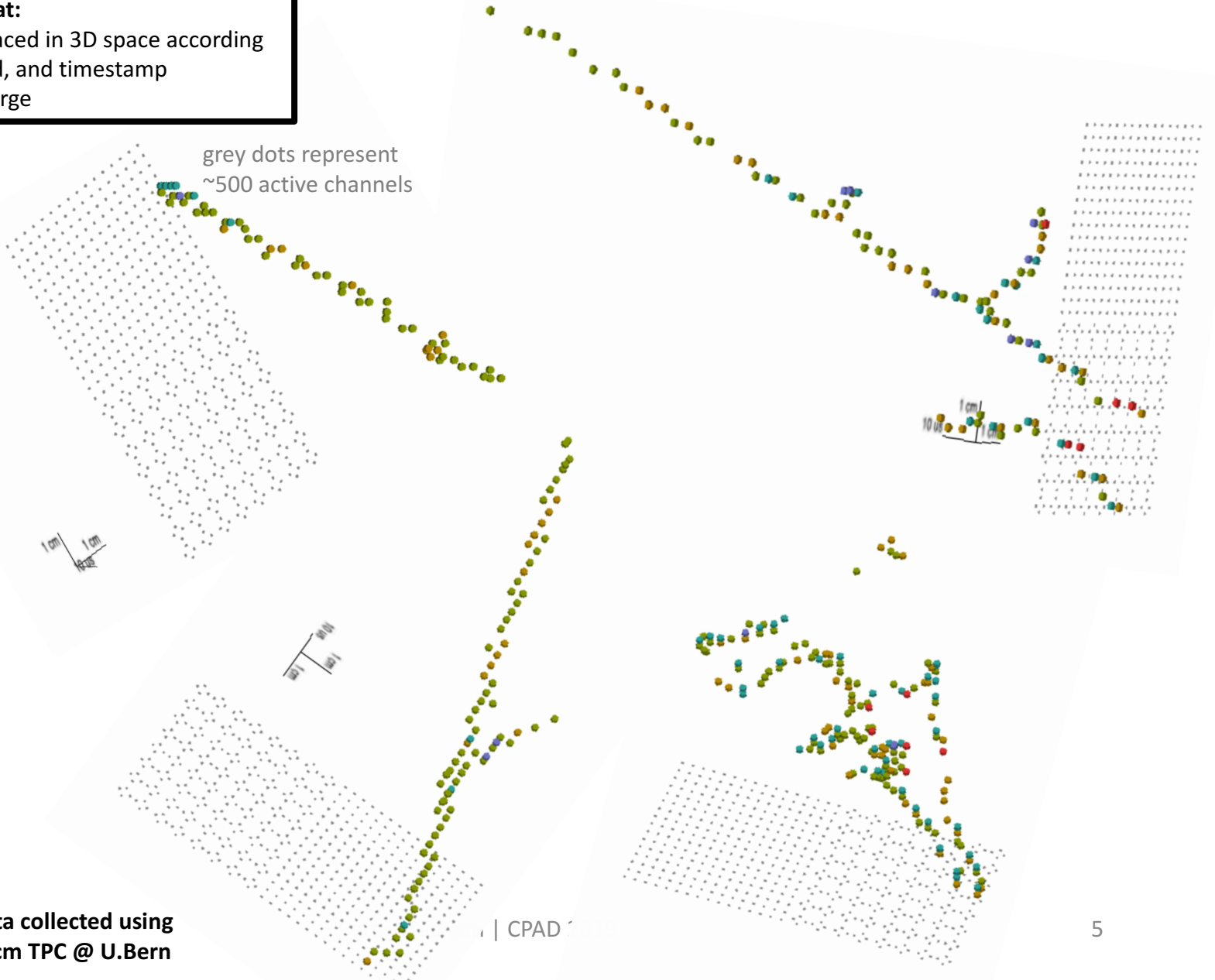
What you are looking at:
- each hit record is placed in 3D space according to chip id, channel id, and timestamp
- color represents charge

ArgonCube

LABORATORIUM FÜR HOCHENERGIEPHYSIK LHEP UNIVERSITÄT BERN

Data collected using 60cm TPC @ U.Bern

grey dots represent ~500 active channels



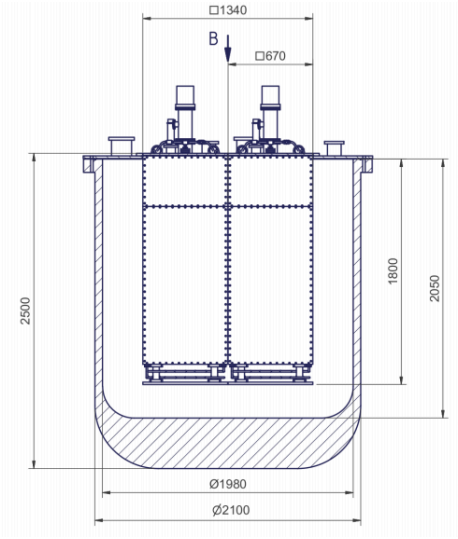
Ton-scale demonstration: ArgonCube 2x2

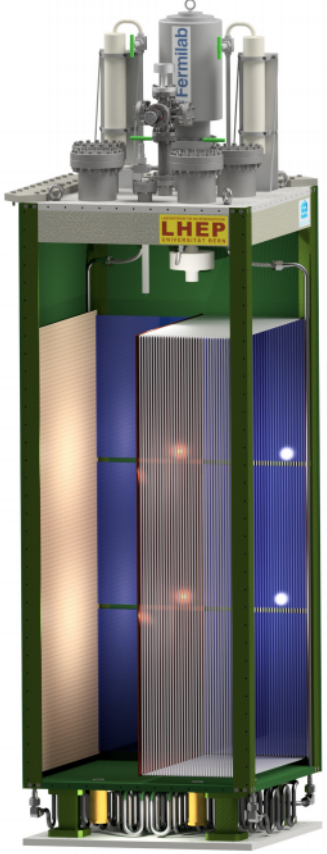
ArgonCube 2x2 demonstrator:

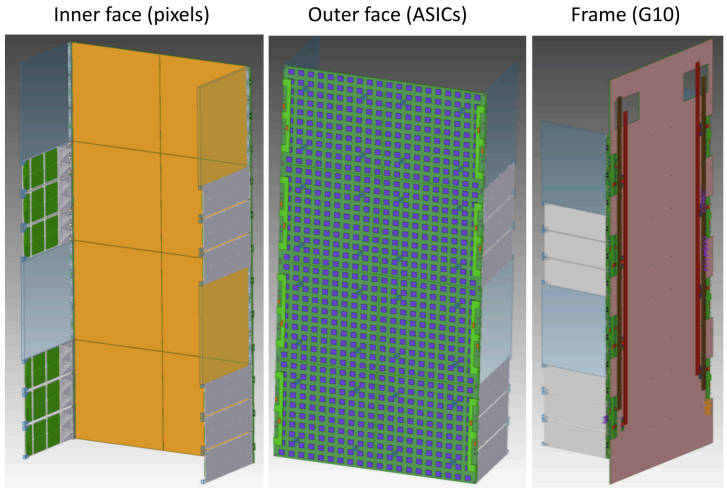
- Engineering prototype for DUNE LAr ND
- To be installed in NuMI beamline at Fermilab
- Planned operation in 2020

Design:

- Modularized TPCs to provide segmented scintillation light
- 4 x (0.7m x 0.7m x 1.3m) modules
- Pixelated readout
- Resistive shell field cage







Anode plane design

LArPix requirements for ArgonCube 2x2:

- Provide 3D charge readout for 4 modules
- 6.4m^2 = ~400k pixels = ~6400 LArPix ASICs
- Robust to single-point failures
- Industry-standard fabrication and assembly to keep costs low

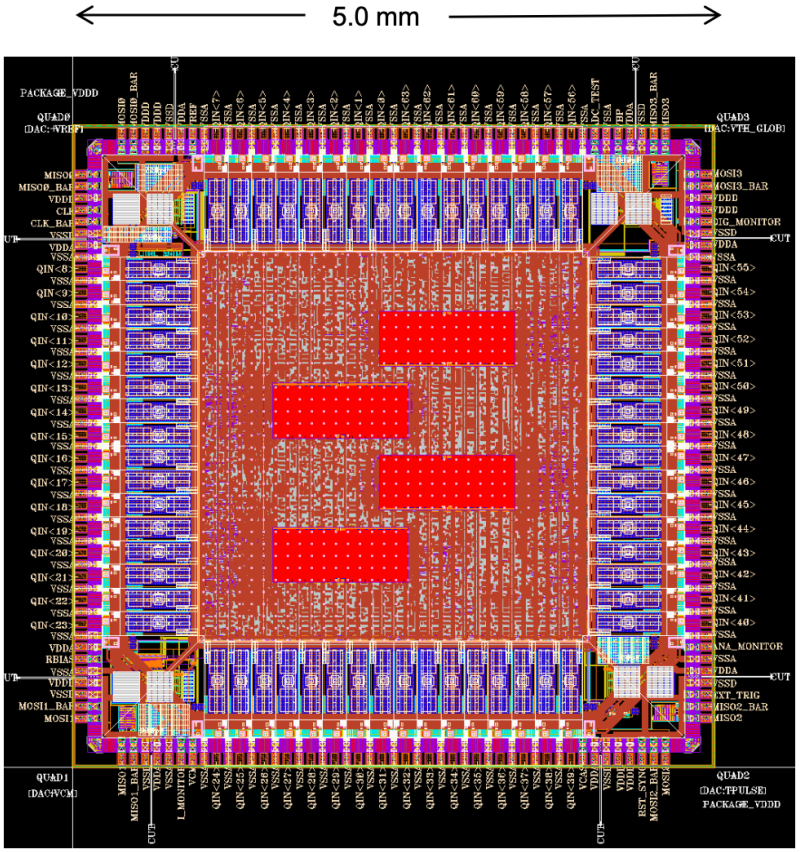
LArPix v2 ASIC

- LArPix v1 demonstrated noise and power targets
- LArPix v2 to determine operating parameters for physics performance

Many additions to optimize physics capabilities:

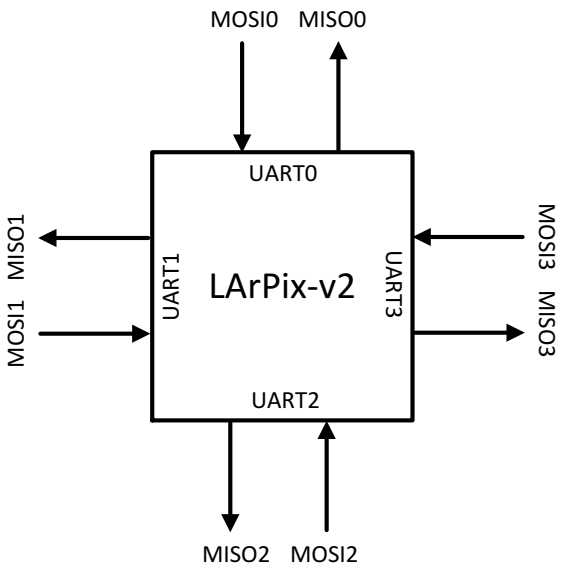
1. Tunable 8-bit ADC
2. Trigger logic modified to reduce dead time add unique trigger modes
3. IO redesign for reliability
4. SRAM memory for larger FIFO depth / less silicon area
5. Tunable internal voltage and current sources for compact PCB layout
6. Enhanced internal voltage and current monitoring
7. 200+ configuration registers to explore performance parameter space

Chip design complete and expect production to be complete January 2020!



LArPix-v2
64 channels, 25 mm^2

Robust communication: Hydra IO



LArPix utilizes a ganged readout structure to limit cryostat penetrations and reduce heat load + complexity

- *IO structure must be robust to single chip failures!*

Hydra IO (concept by D. Dwyer)

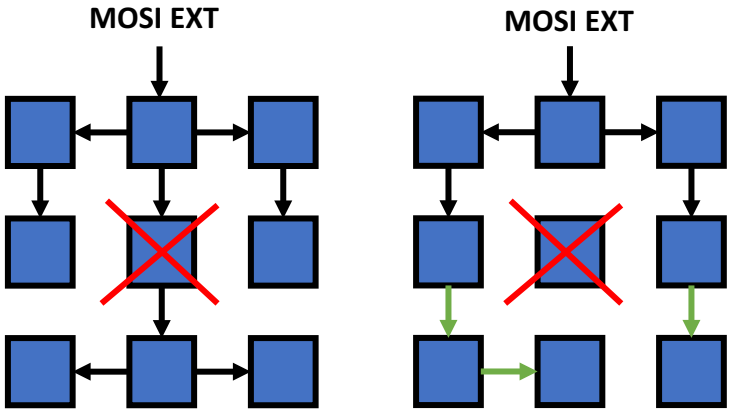
- Each chip acts as a network switch with 4 configurable UART channels

Upstream network:

- Configuration write
- Configuration read request

Downstream network:

- Configuration read response
- Data



Network can be reconfigured to avoid failed ASICs!

Hydra network optimization

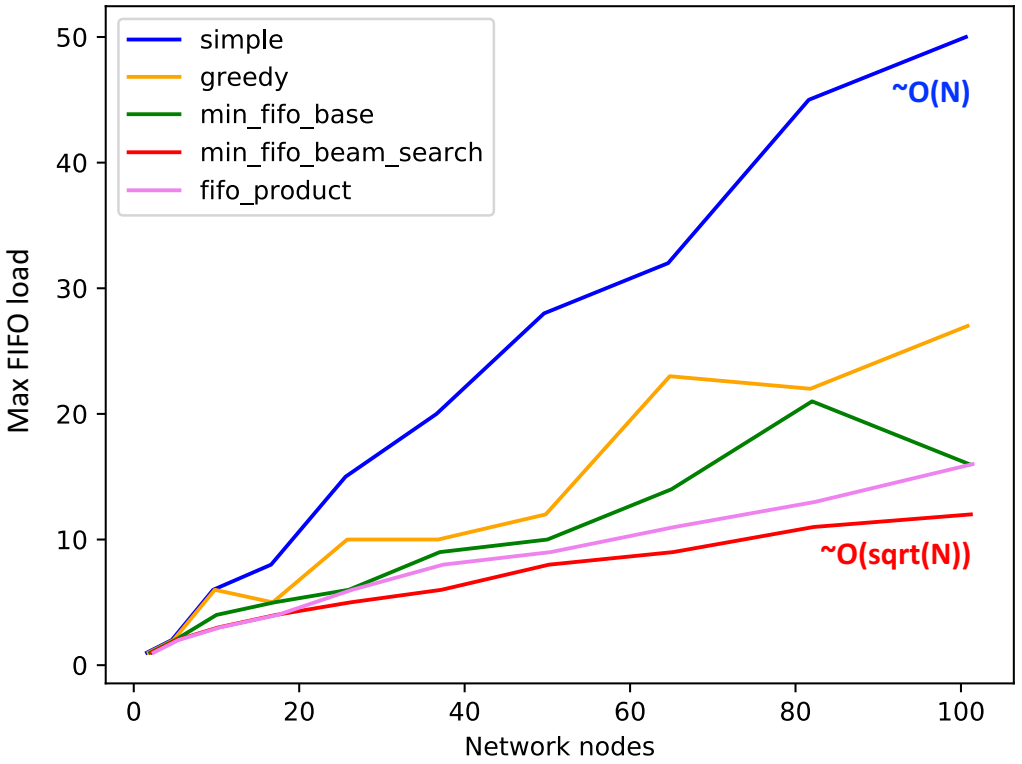
What is the ideal network configuration?

Want:

- Short readout delay
- Low risk of data loss (FIFO usage)
- Minimal digital activity

Developed automated algorithms for near-arbitrary ASIC configurations

- Guarantee shortest readout path
- Minimize proxy metric for FIFO usage during data bursts



For ArgonCube 2x2 and beyond:

- Use a simulation or data driven configuration for baseline network
- If/when ASICs fail, use algorithm to quickly generate alternatives

Cost optimization: SRAM memory

SRAM substantially reduces silicon area for same FIFO depth

CryoCMOS chip

- Designed by LBNL IC design group
- 180nm CMOS cold-model test chip
- Includes 512 x 64bit SRAM memory chiplet

Verified cryo-functionality across LArPix operational regimes (1V-1.8V, 10MHz)

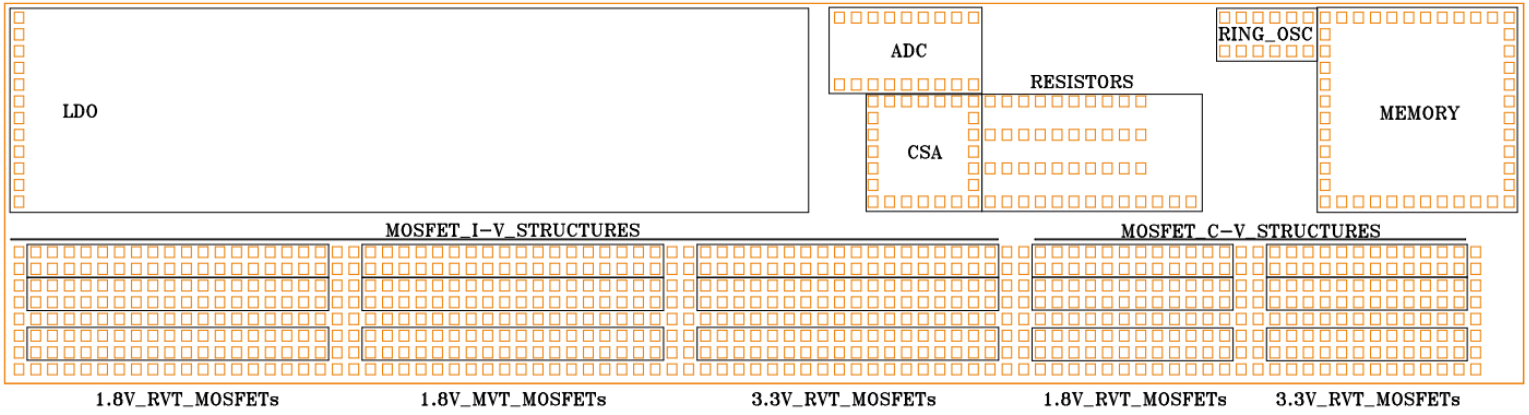
MATS++(cold)	1MHz	2MHz	5MHz	8MHz	12.5MHz
1.8V	0/1536	0/1536	0/1536	0/1536	0/1536
1.5V	0/1536	0/1536	0/1536	0/1536	0/1536
1.2V	0/1536	0/1536	0/1536	0/1536	0/1536
1.0V	0/1536	0/1536	0/1536	0/1536	0/1536

Pattern test (cold)	1MHz	2MHz	5MHz	8MHz	12.5MHz
1.8V	0/512	0/512	0/512	0/512	0/512
1.5V	0/512	0/512	0/512	0/512	0/512
1.2V	0/512	0/512	0/512	0/512	0/512
1.0V	0/512	0/512	0/512	0/512	0/512

Single bit test (cold)	1MHz	2MHz	5MHz	8MHz	12.5MHz
1.8V	0/5120	0/5120	0/5120	0/5120	0/5120
1.5V	0/5120	0/5120	0/5120	0/5120	0/5120
1.2V	0/5120	0/5120	0/5120	0/5120	0/5120
1.0V	0/5120	0/5120	0/5120	0/5120	0/5120

Byte error fraction

CryoCMOS chip padring (LBNL IC design group)

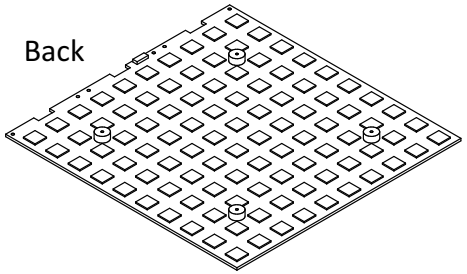


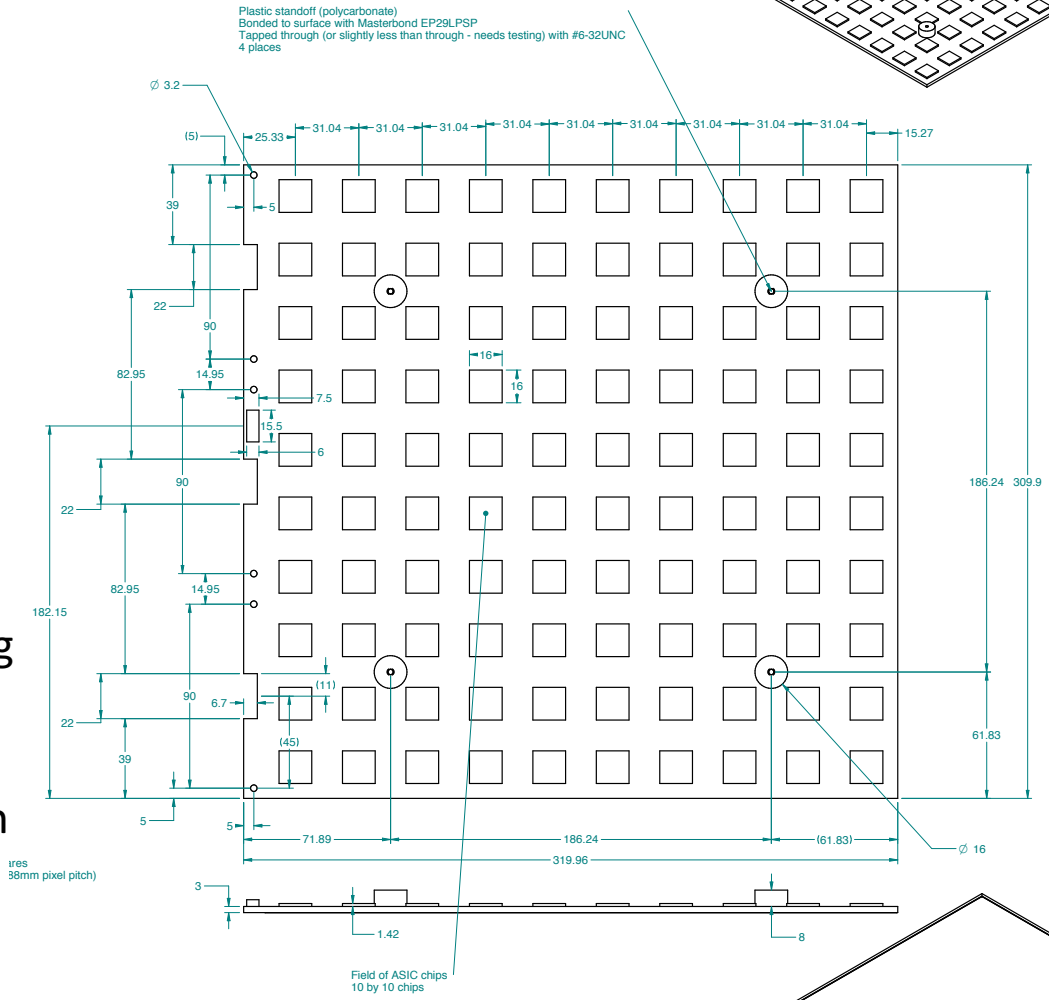
Ton-scale demonstration: Anode design

Cost minimization:
- 30cm multilayer PCB-tile
- Packaged LArPix ASIC

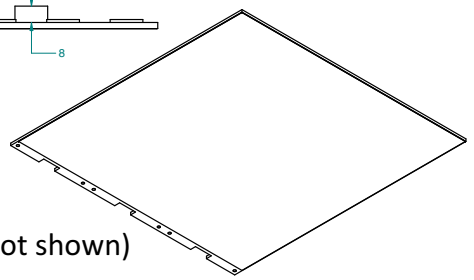
Front:
- 80x80 3.8mm pixel array

Back:
- 10x10 LArPix ASICs
- 4 tapped standoffs for mounting
- 1 cm service edge for routing power, cable interface, and mount points for light collection system





Mechanical design by K. Skarpaas

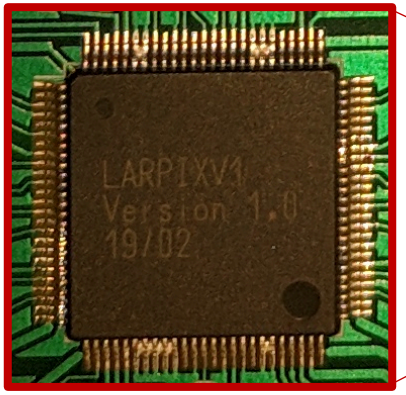


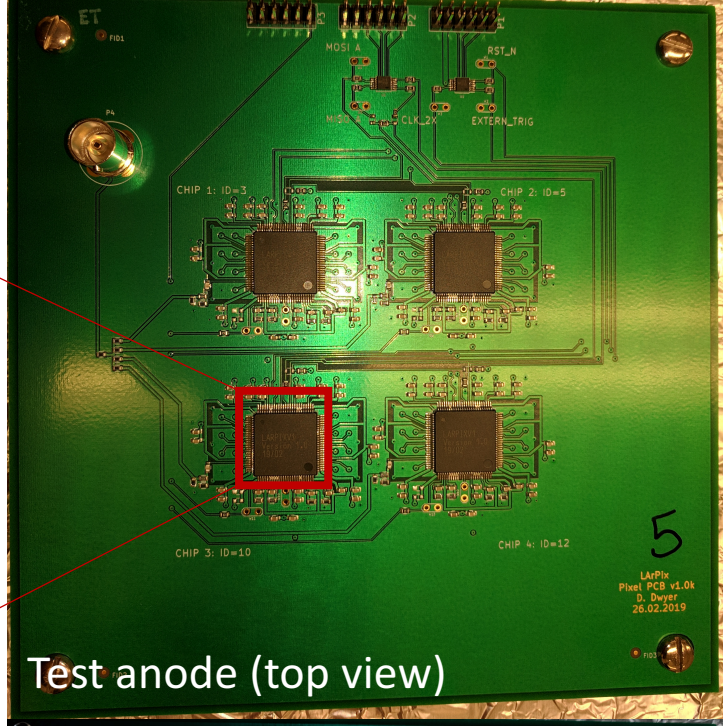
Front (pixels not shown)

Anode design testing

Packaging option:

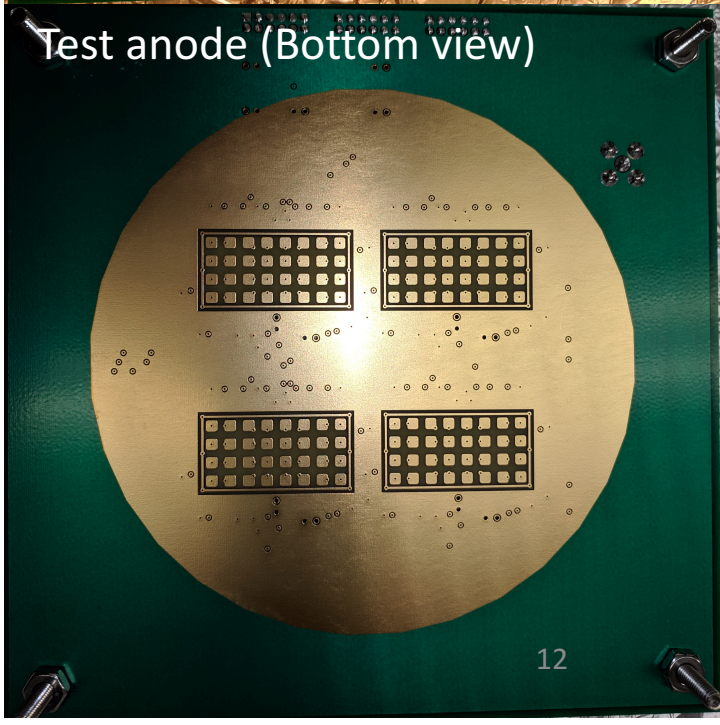
- QFP-100 using existing v1 ASICs
- Looking for packaging yield and cryogenic compatibility





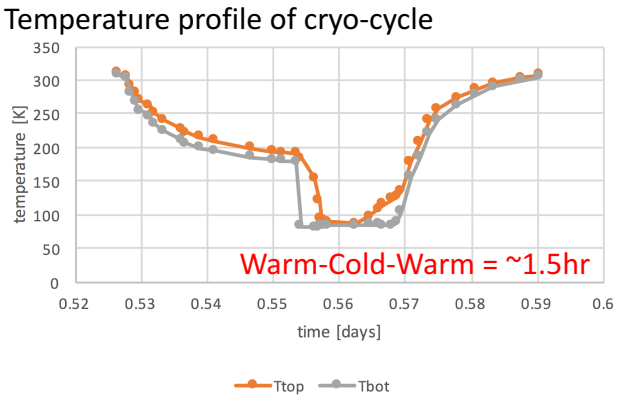
Test anode tile:

- digital + analog on single multilayer PCB
- hosts 4 packaged ASICs
- 30 x (4mm x 4mm) charge collection pads / ASIC
- external test pulse injection circuit on 1 channel / ASIC
- 1 reference channel / ASIC



Combined: Investigate issues associated with packaging, digital-analog cross talk, routing, etc.

Packaging and PCB testing: Yield



Investigated cryo-compatiblity via rapid cryocycling

Standard functionality tests:

- Digital functionality via configuration write and read back
- Analog functionality via standard quantities:
  - Pedestal RMS
  - Noise threshold
  - Leakage current
  - Test pulse response

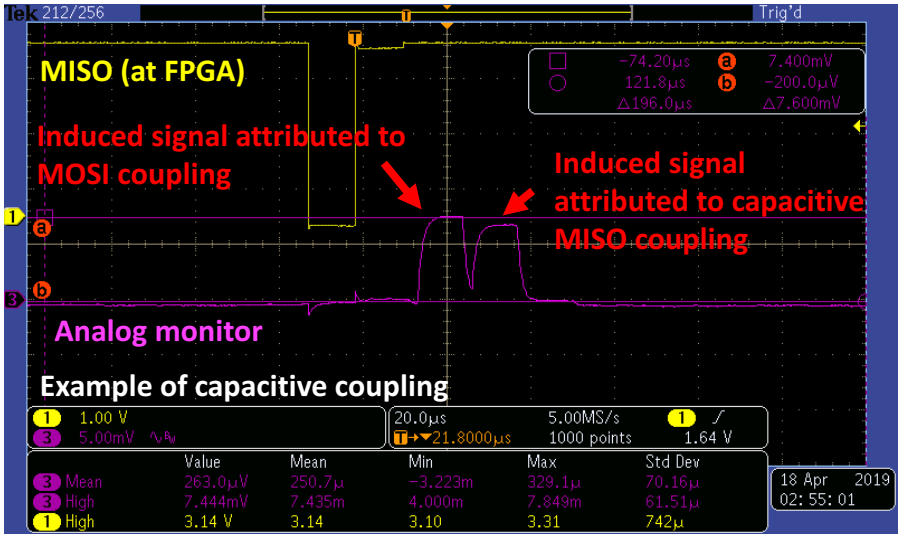
No observed failures associated with cryocycle of packaged ASICs!

Stage / test	Input [chips]	Pass [chips]	Fail [chips]	Yield [chips]
Packaging	158	155	3	98.1%
Assembly	20	20	0	100%
IO functionality	20	19	1	95%
Front-end functionality	20	19	1	95%
Cryo functionality	18	18	0	100%
			Net:	88%

PCB design: Cross talk

Very small capacitive coupling of 10aF-100aF between digital traces and front end can induce O(100) e- eq. pickup

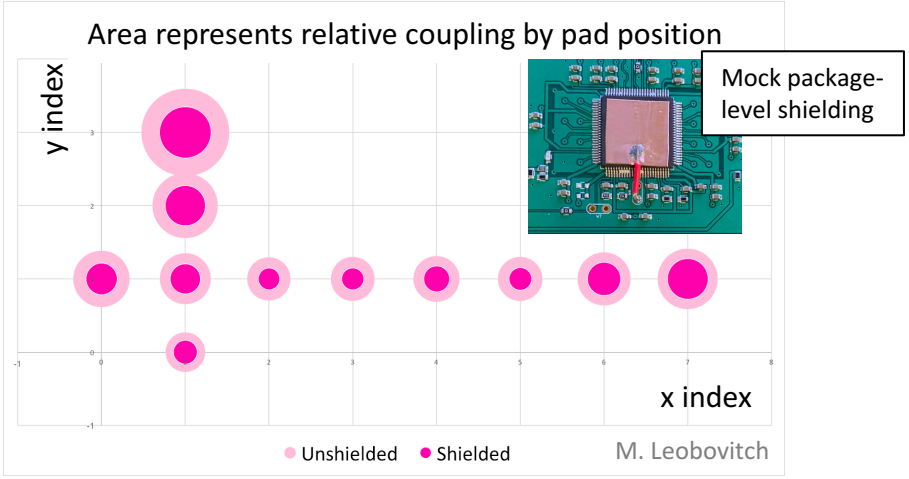
Elimination of stray capacitance to digital traces is critical!



Mitigation techniques:

- Careful routing of digital signals
- Mock package-level shielding demonstrated to reduce coupling by ~2x
- Full anode shielding eliminates cross-talk (e.g. grounded aluminized film)
- Psuedo-differential signaling (v2 ASIC)

Multiple avenues for eliminating pickup!



Packaging and PCB testing: Local induced boiling

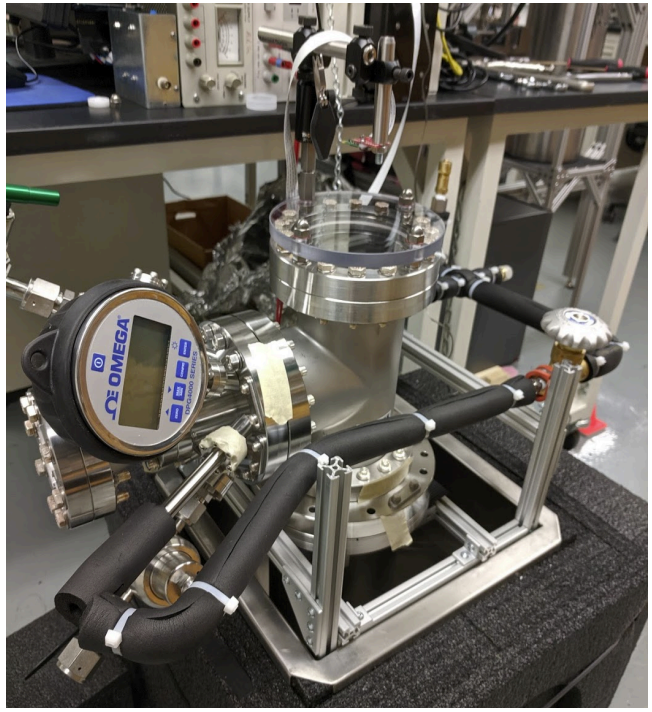
Observe spurious signals when operating chips at high rates and at shallow depths in LAr

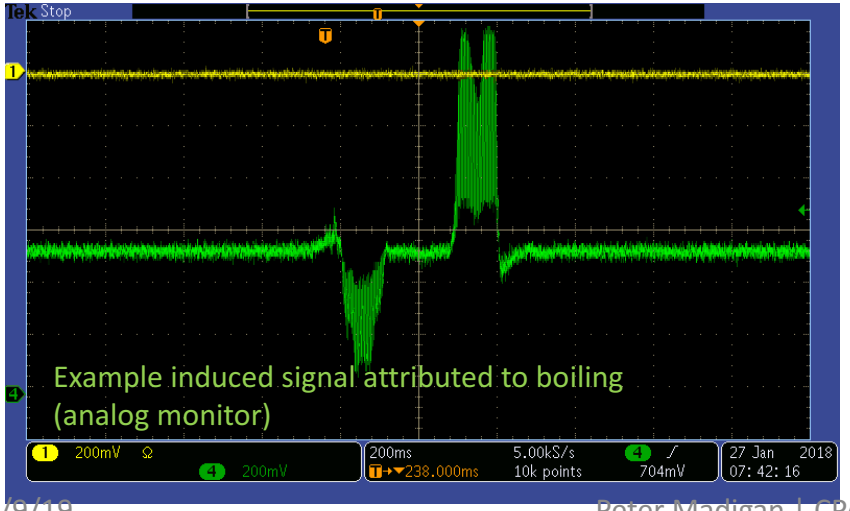
-> attributed to localized boiling of Argon

Building a test stand to directly measure boiling threshold for electronics in LAr

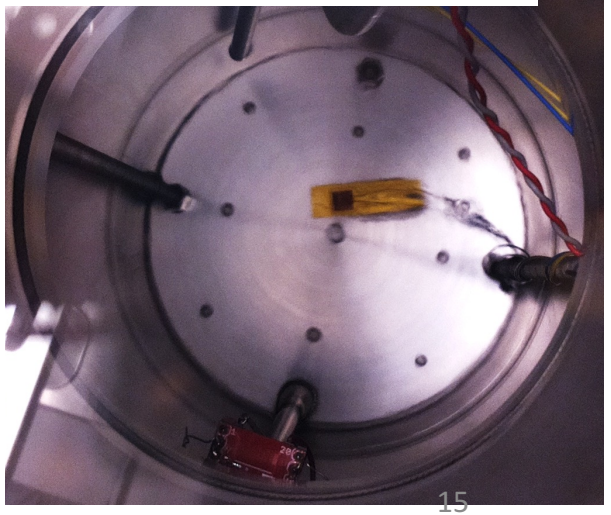
- Pressure stability of ~0.01psi
- Liquid level to sub-mm
- LAr level eq. of 0-5 meters

Test stand commissioned with LN and LAr results expected soon!

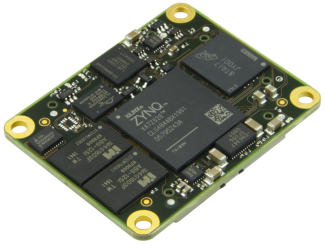




Test chamber during LN commissioning
Boiling on RTD leads can be observed

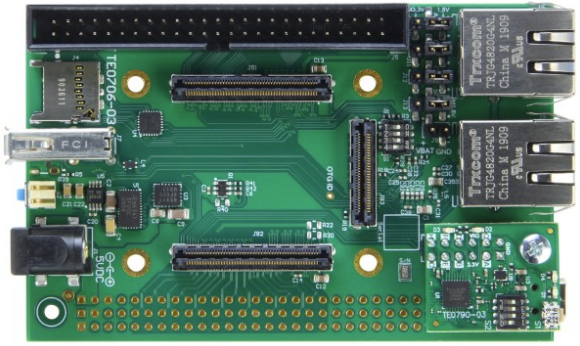


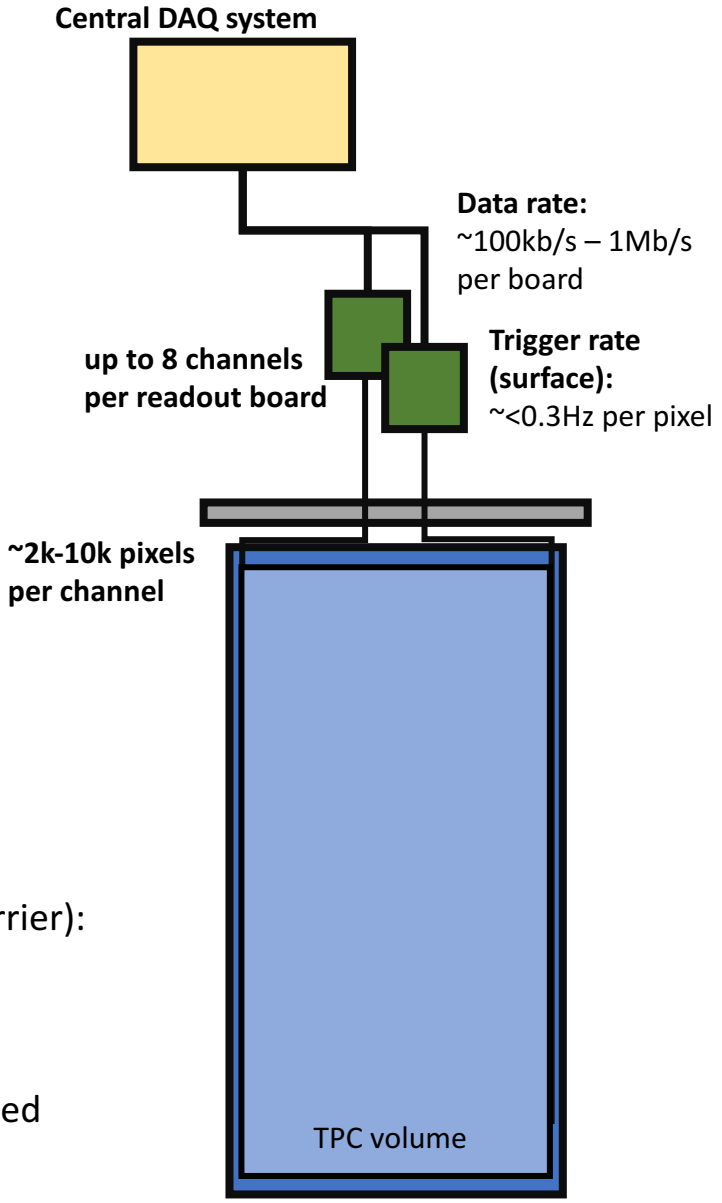
Scale demonstration: LArPix warm readout



TE0702 module

TE0706 carrier card





Buffering and control electronics are required to interface with the rest of DAQ

LArPix v2 readout board (in progress at LBNL, UC Davis):

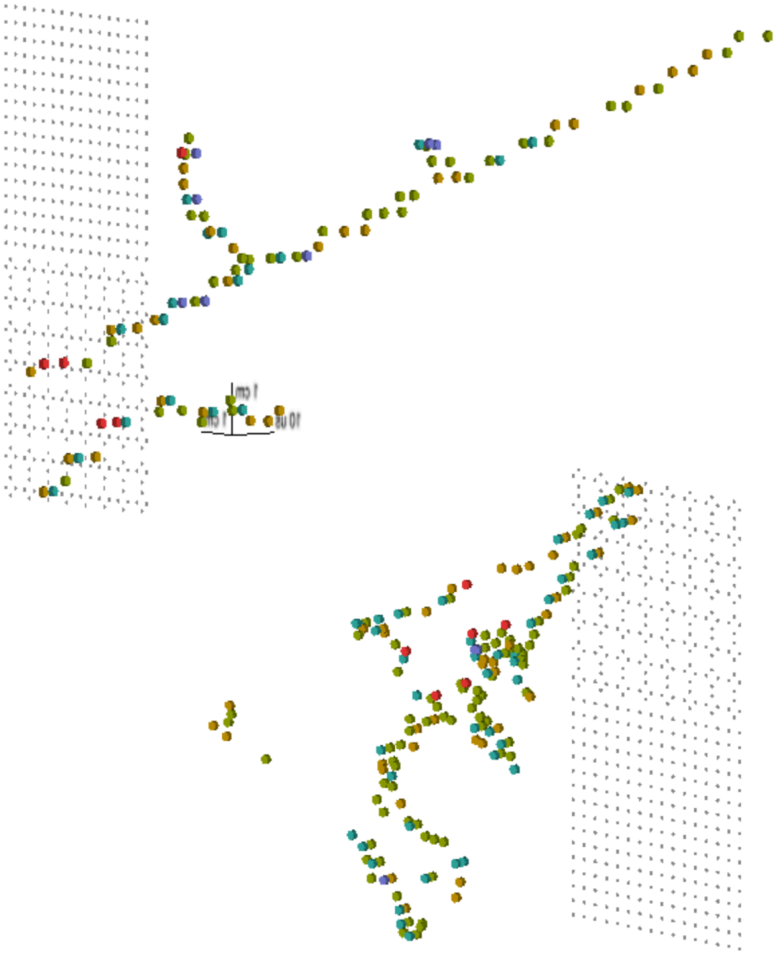
Trenz TE0702 module + custom carrier card (based on Trenz TE0706 carrier):

- low-cost and scalable
- ~Mb/s data rate allows for simple 1Gb/s ethernet
- support up to 8 IO channels for redundancy or high pixel count
- provide analog + digital references, clock, trigger, sync, and integrated ADC

Borrows many design concepts from v1 workhorse board designed by I.Kreslo (U.Bern)

BERKELEY LAB UC DAVIS UNIVERSITY OF CALIFORNIA

Summary and future outlook

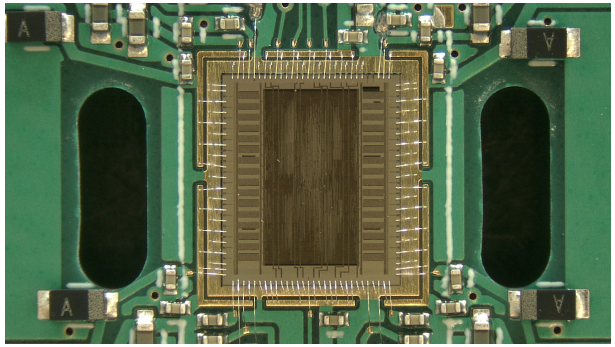


LArPix v1 ASIC demonstrated that LArPix concept meets power and noise requirements

Targeting an ton-scale demonstration with LArPix v2 ASIC in ArgonCube 2x2

- Explored packaging option appears viable
  - No observed cryogenic failures
- Unified digital/analog anode design is possible
  - Requires some mitigation of digital-analog crosstalk
- LArPix v2 ASIC design complete and expecting dies Jan 2020

On track for demonstration of ton-scale 3D charge readout in 2020!



Partners

Team effort to make this possible!

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RUTGERS
THE STATE UNIVERSITY OF NEW JERSEY

UCDAVIS
UNIVERSITY OF CALIFORNIA

Caltech

UC SANTA BARBARA

b
UNIVERSITÄT BERN

Standing weekly meeting and group list serve – let us know if you want to get involved!