Long Term Needs to Maintain IC Development and Implementation

Development of IC design workforce and IC design literacy among Physicists:

In order to stay at the cutting edge of ASIC and Readout Technology for High Energy Physics we need to continuously develop a pipeline to allow talented junior physicists to become familiar with and actively involved in IC design. In particular, we know that students who have participated in actual chip submissions for HEP experiments become physicists who are quite effective in planning, reviewing and designing new detector systems. However, due to the high cost of submissions and the long development time, the center of activity in the area of ASIC development has moved more and more to our labs and only in very few cases involves University groups. The result is that our pipeline of physics graduate students and postdocs able to participate in HEP specific IC design is shrinking. We need to improve mechanisms to keep students actively involved. A number of measures could help. To get hands on experience it would be reasonable to have visitor positions hosted at national labs with HEP relevant ASIC training given by designers working in the field supported by grants from DOE covering ~ 10% of their time. In addition it would be highly valuable to support annual or semi-annual workshops emphasizing digital and analog ASIC design techniques with presentations given by designers and support provided including travel and registration fees for a limited number of US students, post-docs and HEP supported design engineers. To avoid NDA issues generalized technology nodes would be covered without mention of design parameters specific to a commercial company. This would allow students and others with an interest in instrumentation to mingle with and possibly network with members of ASIC design teams. A potentially important way to spread ASIC design knowledge across a broader community would be to support multi-institution FOA's joining efforts of universities and national labs to co-design front end ASICs targeting future detector systems. Smaller institutions could take on verification and testing responsibilities or choose to design specific blocks of an ASIC. Regular ASIC development meetings would serve to distribute the understanding of the issues that need to be addressed in the design of the complex ASICs we will need for the next generation of detector systems. Active participants in these ASIC design FOA's would provide the US community with informed designers ready to help with instrumentation for next generation of large scale HEP detector systems.

Access to future tools and processes:

From its inception in 1981 till May of 2019 ASIC fabrication facilities have been primarily accessible to HEP designers through a fab brokerage service, MOSIS (www.mosis.com), run by the University of Southern California. Recently virtually all HEP institutions involved with ASIC designs utilizing affordable mid-level technology nodes have been refused access to MOSIS services as the organization has turned it focus to the ASIC industry's most expensive & advanced process nodes currently at 22nm and below. To keep up with our obligations to the HL-LHC and liquid noble detectors we have had to turn to Europe for help with foundry access to high utilization, well maintained technology nodes that are less expensive and serve our signal and data processing needs more appropriately. While it is good to have alternatives, this experience points out the fragile position that many US research communities are in that require Application Specific Integrated Circuits to advance their work. This potential lack of access to foundries and importantly their technical descriptors (PDK's) is perhaps the biggest threat to maintaining US world leadership in front end readout capabilities for tracking and calorimetry.

Most HEP experiments are implementing designs in 130 & 65nm nodes with 28nm recently gaining support from CERN for its potential for use inner tracker sub-systems. This

exploitation of moderate cost technologies appropriate for the purpose of advancing our science objectives ultimately allows the community to maintain a broad scope of experimental objectives that maximize our discovery potential.

Multi-Institution Agreements - The design of integrated circuits has evolved significantly over the past 30 years with feature size going from 10's of microns to 10's of nanometers and documentation increasing in inverse proportion. At the same time HEP integrated circuit designs have grown from single purposed functional blocks with a few hundred transistors to systems on a chip with many different blocks supported by more than a hundreds of million transistors in sophisticated pixel tracker designs. These designs require the coordinated effort of a broad range of experts resulting in a large team designers drawn from multiple institutions. For the CERN upgrade we have had the benefit of a "frame contract" allowing collaboration between universities and labs who sign multi-institutional NDA's designed to allow the size of the design team involved with the development of our complex readout chips to be expanded beyond institutional boundaries. In the US the demise of access to MOSIS brokeraged fab and their support for technology based design kits along with increasing foundry restrictions on sharing IP it is becoming nearly impossible for groups to share IC design tasks among HEP institutions. In order for the US to maintain its competitive world leadership position in the development of instrumentation for High Energy Physics we need to solve this issue.
The CERN frame contract with TSMC was put together and managed by IMEC an R&D firm based in Belgium, founded in 1984 to perform R&D in nanotechnology and provide brokeraged fabrication services to small research and business communities. As many US groups know IMEC has a long history similar to MOSIS, brokeraging wafer fabrication, providing participating institutions with technology specific design kits and taking responsibility for submission of compiled wafer level designs to foundries they deal with. In addition their proven experience in negotiating the CERN frame contract puts them in an ideal position to do the same for US institution. In recent discussions with their US representatives we have learned that IMEC would consider setting up a multi-institutional NDA with their main fabrication partner, TSMC. Regardless of whether IMEC or another intermediary organization is able to do this *we should consider a multi-institutional agreement that allows HEP researchers to collaborate on the design of the next generation of custom integrated circuits an important enabling Research Priority.* Help with the infrastructure required to do this from governmental agencies may be critical in accomplishing this goal.

Important Technical Development to Enable Breakthrough Innovation

The following list of topics is quite broad and our group realizes that resources will allow only some of these topics to receive funding. We envision a multi-topic ASIC Instrumentation FOA that covers most or all of the areas listed below as a way to let the community decide through their proposals where to put critical funding resources.

Cold Electronics for Liquid Noble detector systems:

Important progress is being made on low power immersed Liquid Noble (LN), cold electronics. Systems designed for these environments (-170C and lower) need good transistor models that are unavailable from ASIC manufacturers and need quality assurance to guarantee reliable performance over the decadal lifetime of an underground experiment. Front end ASIC readouts for underground ionization and photo-electric sensor readouts currently under development should be continued as well as peer reviewed new developments will need new support. A second significant issue has to do with high reliability, low power DAQ

communications ASIC to ASIC, board to board and sub-detector to warm DAQ. Support to focus on these issues should be given to groups planning developments that result in deployment of moderate sized readouts in LN detectors so that relevant experience necessary to mature readout designs that will need to be sustained for the lifetime of large underground experiments can be acquired.

ASICs for Cryogenic Applications:

Investigation of suitable IC fabrication processes, transistor models, library characterization, and design for 4K and below. The HEP applications of interest include readout and multiplexing of sub-kelvin sensors, such as TES and MKIDs, for CMB bolometers of Dark Matter detection. This is also an emerging need in QIS for qubit readout, which does not scale to large number of qubits without cold electronics. There is therefore significant synergy with QIS work. Reduced radiation sensitivity techniques and technology: ASICs for particle physics will continue to apply technology well outside the commercial operating conditions. The extreme track density, data rates and radiation levels in the inner layers of detectors are already a challenge at the HL-LHC. For example, the radiation hardness design goal for the RD53 chip is 500 Mrad total ionizing dose, achieved using a 65nm CMOS process. Rates and radiation levels are expected to grow significantly at future high rate hadron colliders, requiring detailed understanding and continuous development. An immediate PRD recommendation is to explore radiation sensitivity of deeper node technologies (e.g. 28nm) for detector applications. A significant RD effort is needed to make adequate progress on the time scale of 5-10 years.

Picosecond High precision timing:

Studying rare processes in greater detail requires ever-increasing beam intensity and collision frequency. Physics reach is often limited by our ability to make sense of data when events overlap and occupancies are high. Timing information, has long been an essential background reduction technique in high energy physics experiments. Future experiments will require detectors capable of sub-ns time resolution. Fast timing is a rapidly developing new direction for HEP detector instrumentation that provides an independent dimension to particle tracking. Significant RD is still needed to achieve required timing resolution below 30ps meeting at the same time area and power constraints. RD areas of interest within this topic are:

i. Low power CMOS, bi-CMOS readout technology
ii. Low power circuit techniques for timing extraction
iii. Novel pixel based highly segmented readout architecture for position and timing extraction.

Standalone and 3D-integrated MAPS:

MAPs are an enabling technology for tracking systems at future colliders. For linear colliders, the stringent material requirements and segmentation necessitate a monolithic solution for the sensing element and readout ASIC. For future hadron colliders, the size of the planned trackers 500m^2 and tracking calorimeters 5000m^2, the desired resolutions and material makes MAPs the economically and technically viable choice; for hadron machines the total irradiation would pose a difficult challenge requiring further development . In order to maintain the US's historic leadership in tracking systems, a coherent US program of study is urgently needed in order to compete with existing European and Japanese programs. These devices are fully integrated. Sensing, FE, readout and system elements will need to be considered as a whole from the beginning and fabricated in a commercial integrated circuit process obsoleting the costs of interconnect and assembly between sensor and readout and likely eliminating cost of specialized sensor technologies. MAPS designs will encourage close collaboration between sensor and readout specialists whose designs will reside on the same silicon substrate. The differences in the needs for linear collider and future hadron collider for readout rate, radiation hardness and power limitations would require development of independent solutions.

On-Detector Processing for Low-Power, High-Performance Sensor Readout:

Monolithic sensors and readout circuits are continually becoming denser and faster with each new technology generation. Denser circuits allow improved raw performance and enhanced functionality (such as smart pixels). However, the practical achievable density in integrated circuits is limited by power dissipation, and data transport is a key driver for power dissipation. Moving a bit of data off-chip for processing is up to two-orders of magnitude less efficient than performing data reduction on the sensor itself. The most straight-forward way to address the problem of too much data is to not send it in the first place. This is the key benefit of on-detector processing. By not sending as much data, detector speed and functionality can increase. By extracting salient features of the data and sending those out for further analysis the detector takes on an enhanced role in the system.

Traditionally, complex integrated digital signal processing functions have required teams of highly skilled specialists to implement. This barrier to the adoption of on-detector processing can be overcome by harnessing new advances in application-specific, reconfigurable computing. By matching the hardware to the application, power dissipation can be reduced by orders-of-magnitude, or equivalently, performance can be increased. Furthermore, by using emerging design tools that allow customization of processor instruction sets, the complexity is largely moved from hardware to software where physics domain experts, rather than integrated circuit engineers, can take the lead in implementing advanced signal processing algorithms. Harnessing public domain resources, such as the RISC-V instruction set, can make moving to on-detector processing significantly cheaper than deploying custom digital logic, an important consideration in future detectors. Another key additional advantage of leveraging software-based algorithms is that reconfigurable computing allows the data reduction to be matched to the experiment, even if the sensor is built. This is an important consideration when amortizing development costs over multiple experiments is necessary.

By relaxing challenging power dissipation and data communication speed constraints, On-Detector Processing can be an enabling technology for advanced MAPS-based sensors, improving both circuit density and performance.

Power Management and Conditioning:

As ASIC technologies have moved towards smaller feature sizes the channel count has increased and both Analog Signal and Digital processing have become increasingly complex. An important side effect of this decrease in feature size is that supply voltages have been getting lower and current requirements increasing while the power density is remaining the same or getting smaller. In order to also minimize the material budget experiments have turned increasingly to DCDC conversion, locating DCDC converters on the same board often as the front end electronics Providing input power with a voltage 10X higher than the front end ASICs require proportionally reduces the cross section of copper by the same fraction a huge win in material reduction. While there have been a few attempts to put a DCDC conversion on the front end ASIC, so far none has been successfully implemented in an experiment. While the micro-electronics community has been publishing successful on chip DCDC conversion techniques since the turn of the century. As reduced feature size drives core voltages even lower it will become increasingly necessary to implement efficient power conversion on chip in world class designs. Support for the development of DCDC conversion techniques that are documented and available for unfettered use is a significant PRD to enable next generation designs of high density front end ASIC readouts.

Wireless Communications:

Wireless Communication is a mature electronics technology not yet exploited in HEP detectors. Bluetooth as an example is already ubiquitous in the Internet of Things. Instrumentation, and technology currently exists in IC form using chip antennas. A simplified adaptation for slow control and monitoring applications in HEP would serve to un-clutter high speed physics data communications and could be a stepping stone to next uses where trigger or other event related data could be transmitted independent of a wired control path.

High speed Data transmission interfaces :

Copper links and encoding - Within a few years of the start of the HL-LHC Phase II running the inner layers of the CMS and ATLAS pixel trackers will need replacement due to the extreme radiation environment. New technologies offer the opportunity to significantly improve the bandwidth of communications links of these layers presently limited to less than .5GHz if RD funding is made available soon. Bandwidth improvements in cables and potentially radiation tolerant ASIC technology (such as PAM4) make it possible to consider 5X improvement in data transmission over copper links to areas of the detector where radiation levels are low enough to allow a switch to sufficiently rad tolerant 10Gb optical links presently under development to carry the data to the readout areas.

Silicon Photonics - Optical transmission standards in industry are very advanced, now getting to 400Gbps links. There is a large impedance mismatch" between industry and HEP needs. In addition to radiation tolerance and low mass, HEP data sources in a detector are not concentrated at one point, as suitable for very high speed links, but distributed over cubic meters of volume.. Adaptation of silicon photonics technology, such as wavelength division multiplexing is needed to meet HEP needs. Such out of the mainstream use cases could in turn meet commercial niche application needs.

AI and neuromorphic and asynchronous Readout Techniques:

Machine Learning (ML) and Artificial Intelligence (AI) systems are already changing the way large data sets are interpreted, increasing the potential for discovery of current experiments. Currently, sequential processors (requiring multi-GHz clocks) and general purpose new generation FPGAs are the main vehicle for implementing such type of systems with some inherent limitations. We can expect ML and AI to have more powerful impact when these systems will operate in-situ or on hardware units optimally designed to implement neural networks, neuromorphic processing and asynchronous techniques.

Two directions are distinguishable: First, the study and development of machine learning programmable ASIC (FPGA-like) with architectures optimized for solving HEP-related problems: in-hardware implemented teaching methodologies, weights calculation and back propagation, and algorithms. And second: detectors capable of extracting high level abstract information from the received signals. This can be achieved through the interplay of in-hardware simultaneous multi-channel processing and resulting in transformation of data in physics information.