Status and Plans of the CMS HGCal Upgrade

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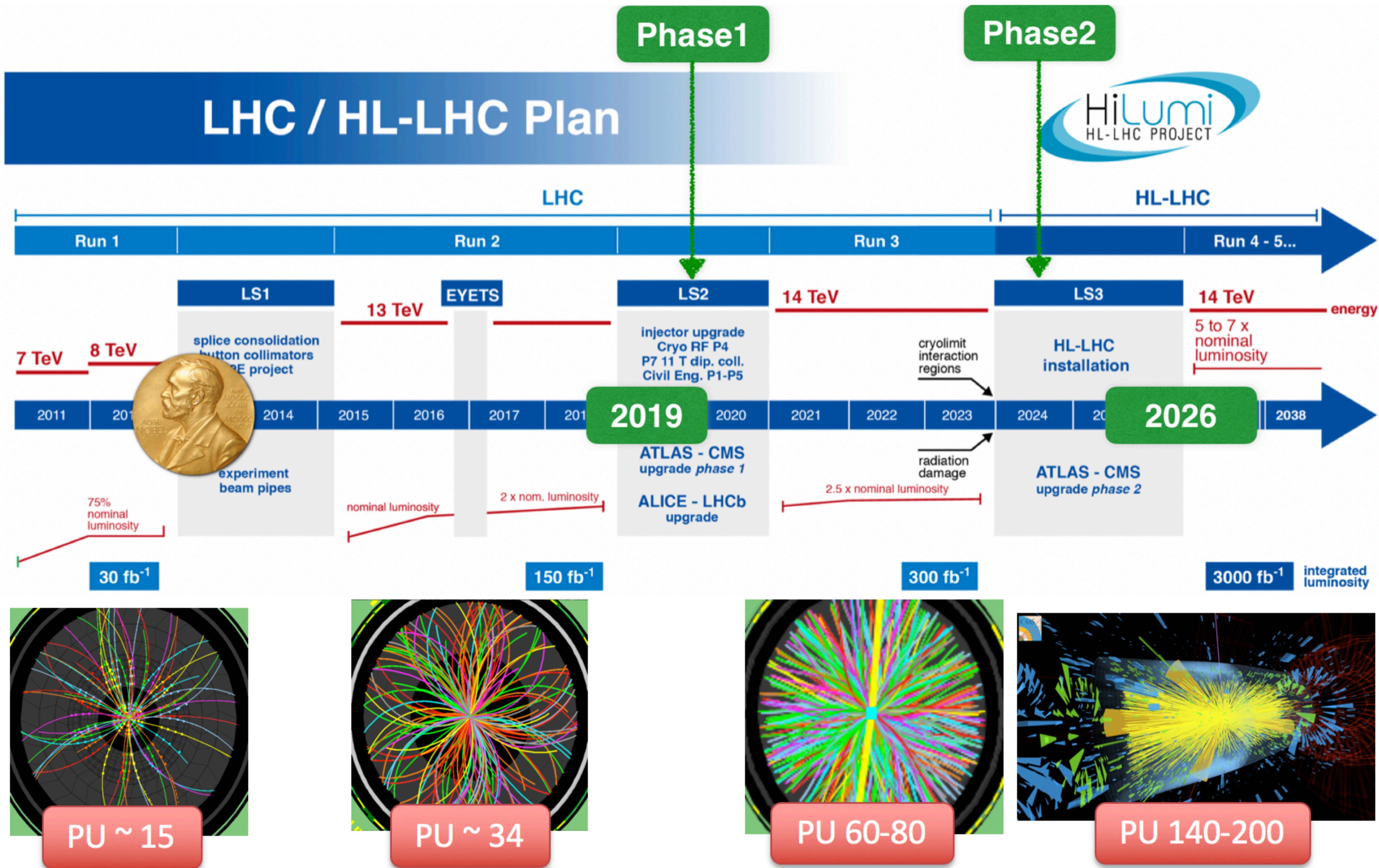
Fermilab

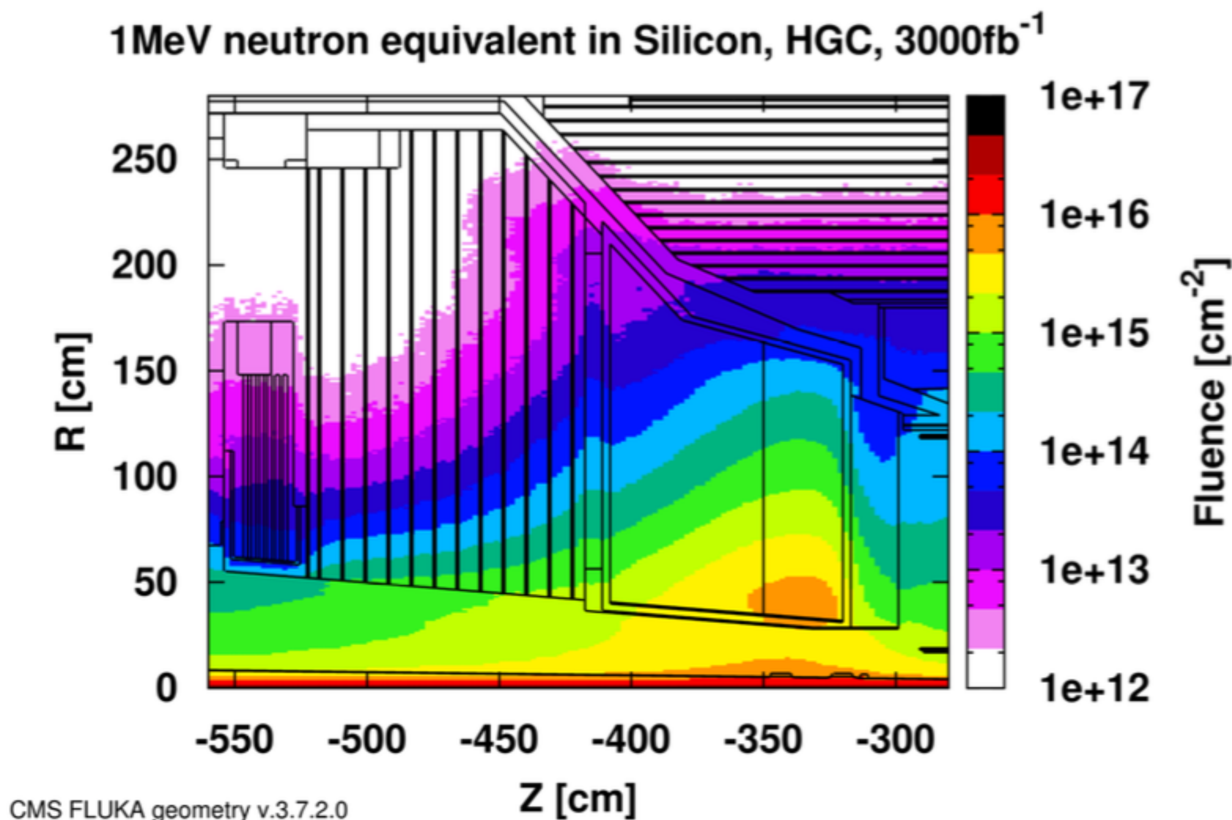
CPAD, Dec 10, 2019

The High Luminosity LHC

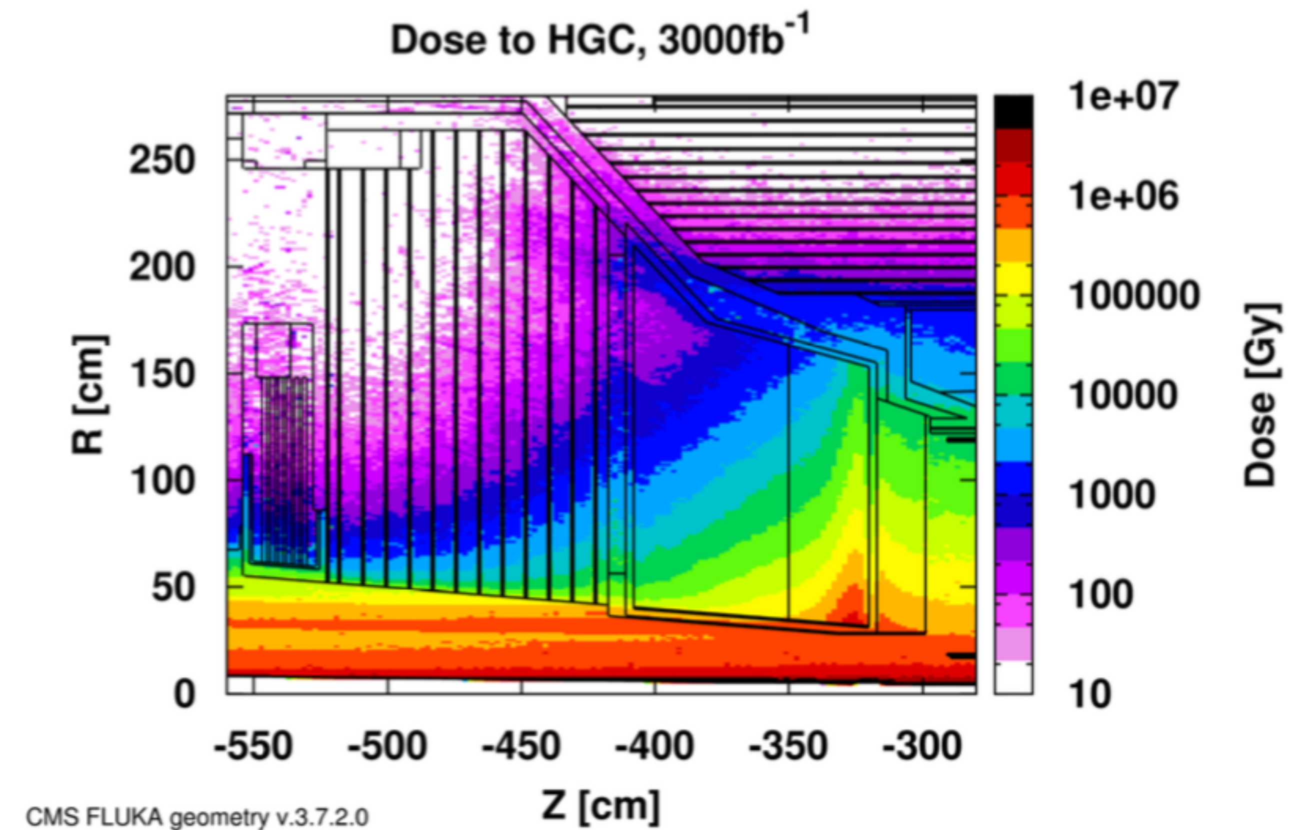


Radiation Challenge

- After the HL-LHC upgrade, the CMS end-cap will operate in an unprecedented **radiation environment**
  - Fluences of up to **10^{16} neq/cm²** and doses of up to **1.5 MGy**
- Will need very radiation hard detector material and readout
  - Strong dependency on |η| and |Z| suggest that **design can vary with exact location**



expected hadron fluences

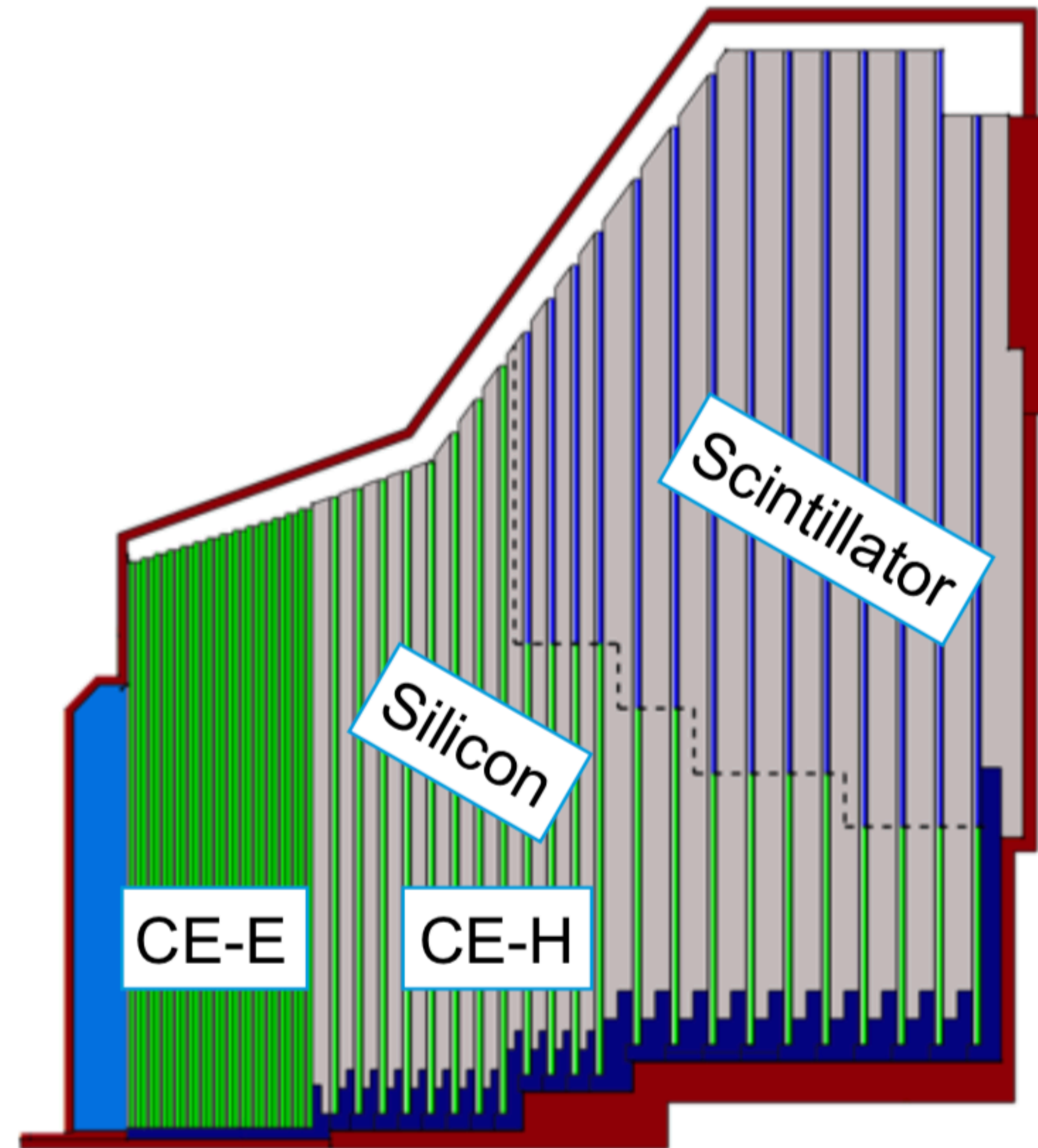


expected total dose

Technology Choices

Both endcaps	Silicon	Scintillators
Area	~620 m^2	370 m^2
Channel size	0.5 - 1 cm^2	4 - 30 cm^2
#Modules	~31000	4000
#Channels	6.1 M	240 k
Op. temp.	-30 °C	-30 °C

Per endcap	CE-E	CE-H (Si)	CE-H (Si+Scint)
Absorber	Pb, CuW, Cu	Stainless steel, Cu	
Depth size	25.5 X_0, 1.7 λ	9.5 λ	
Layers	28	8	14
Weight	23 t	205 t	

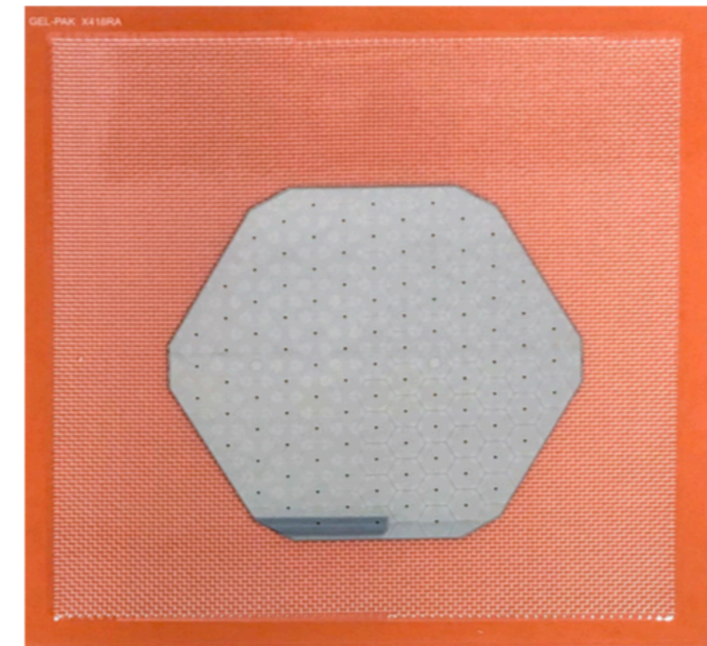


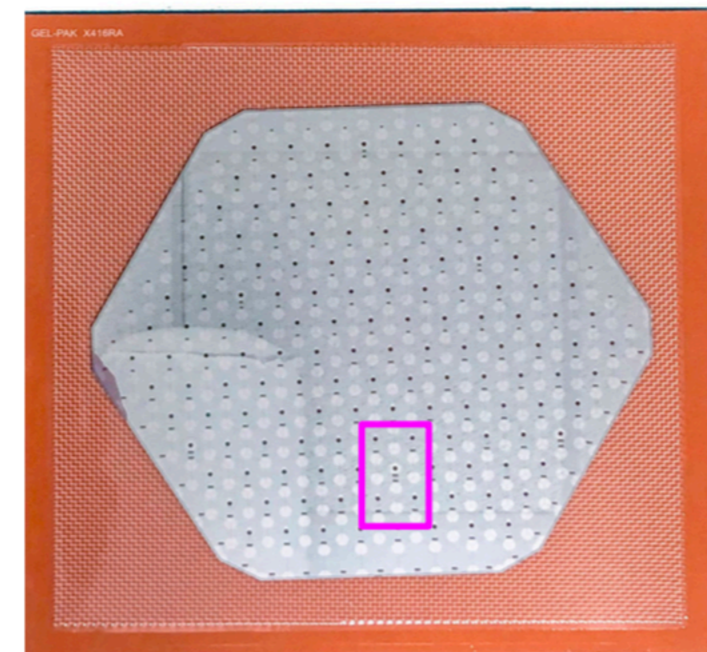
- **Dissipated power ~250kW**
- **Removed with two-phase CO_2 cooling operated at -35C**

Silicon Sensor Layout

- **Hexagonal** sensor geometry as largest tile-able polygon
  - Maximize use of circular wafer
  - Minimize ratio of periphery to surface area
  - Truncated tips (“mouse-bites”) used for module mounting to further increase use of wafer surface
- Calibration cells (small area) to guarantee the ability to achieve MIP calibration

- **8” vs 6” silicon wafer**
  - 8” advantages:
    - Reducing the number of modules
    - Simplifies module mechanics
    - Lower cost
  - 8” disadvantages:
    - Standard deep-diffused Float zone (dd-FZ) wafer material is not available on 8"
    - Production process is new





Hexaboards and Module Assembly

Hexaboard houses up to 6 HGCROCs

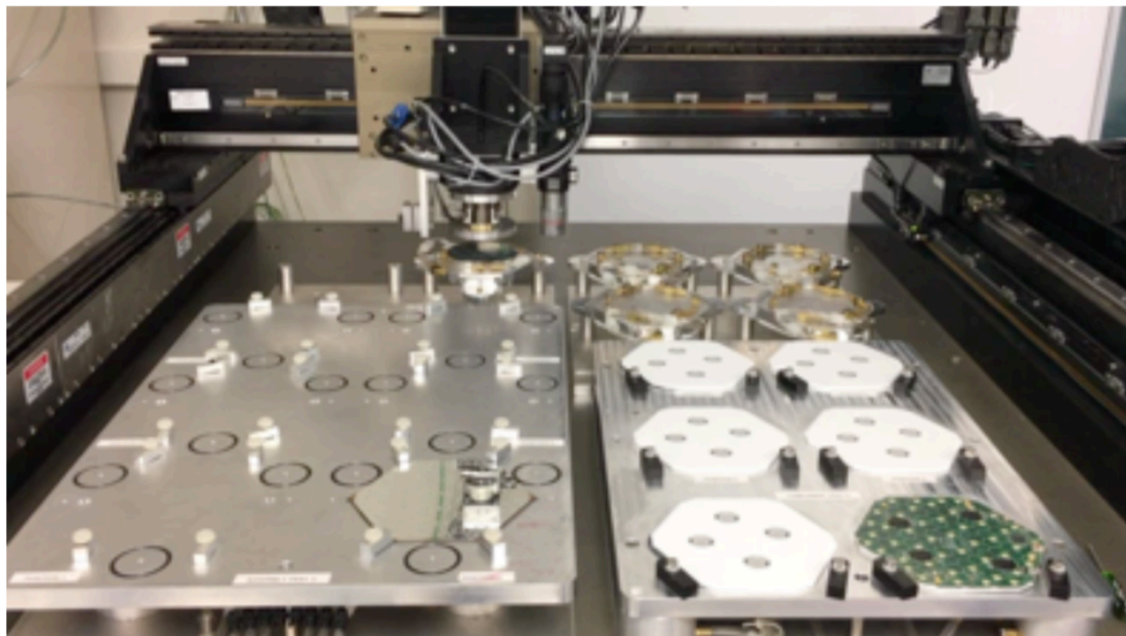
bonding to sensors through holes in PCB

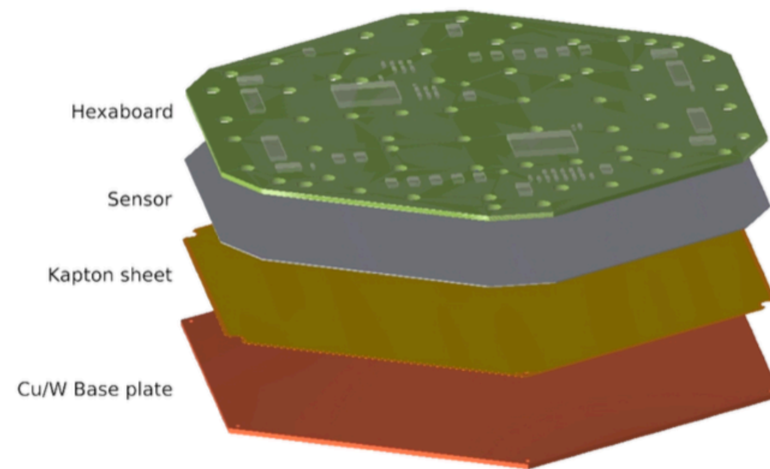
Status: 8” board with HGCROC-V2 in production

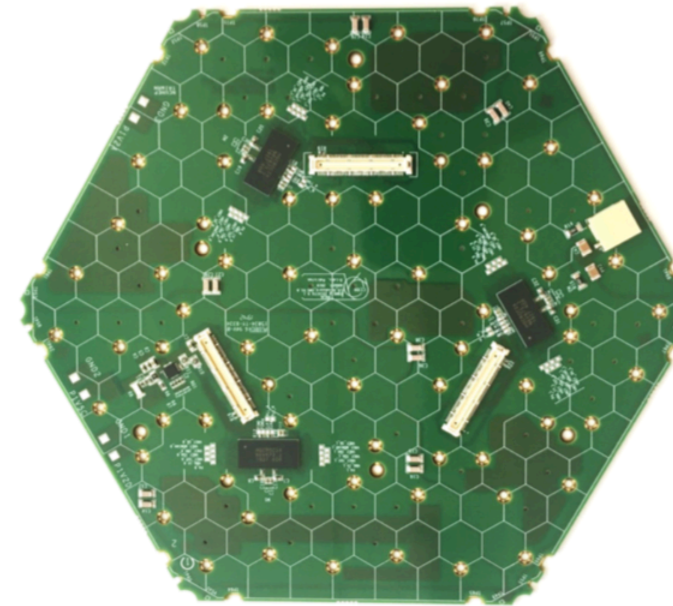
Lead Module Assembly Centre (MAC)

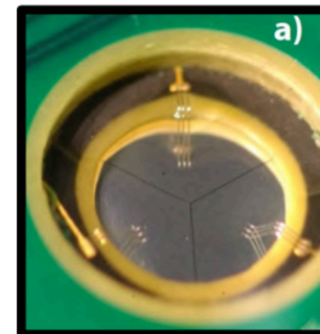
automated gantry at UCSB set up

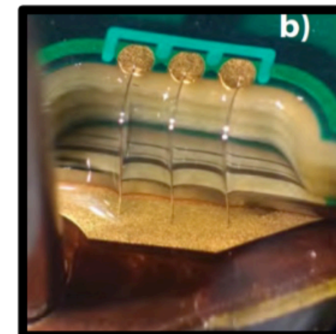
6 MACs world-wide in preparation

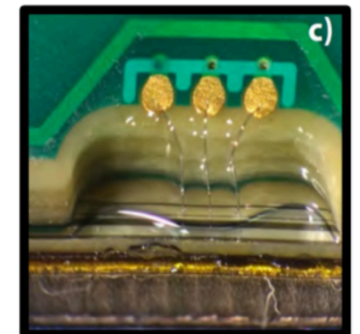


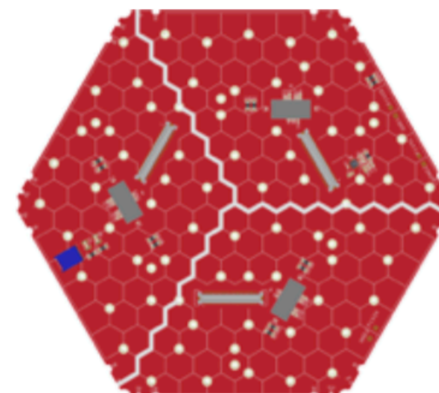


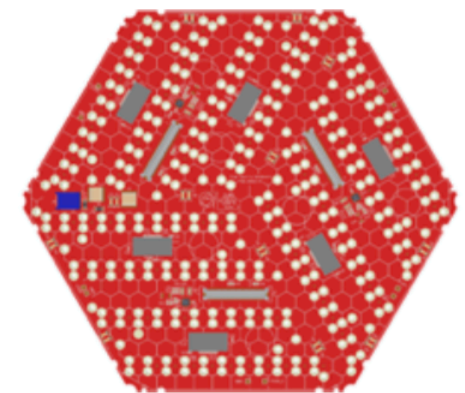












Scintillator Tiles and SiPMs

Extensive studies to establish radiation hardness of scintillator materials and SiPMs

Sources, reactors and in-situ

Scintillator signal loss < 50%

use cast PVT material in inner region

moulded PS based tiles outside

Tile geometry and wrapping optimisation

using test beam and simulations

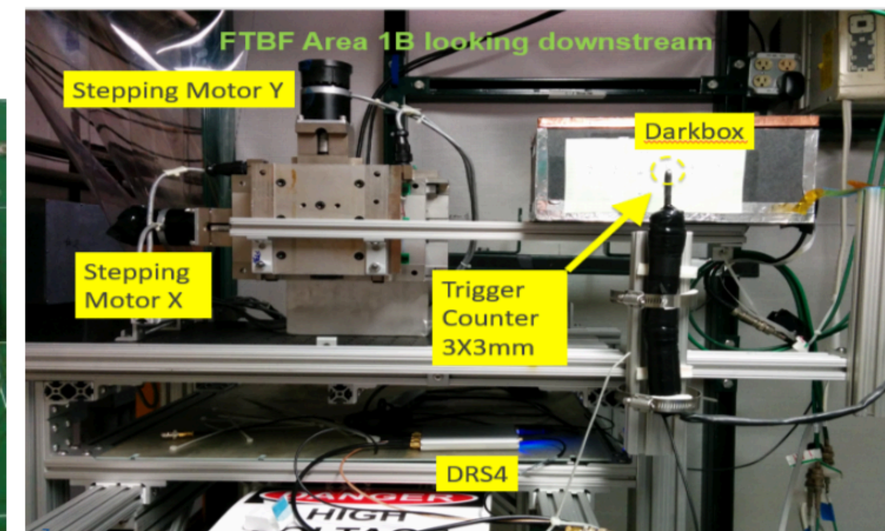
SiPM custom design developed with producers

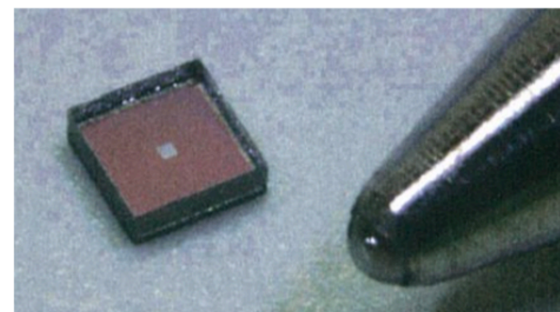
thermally conductive package, rad-hard window

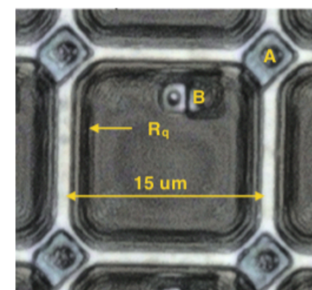
prototypes under way - equivalent devices characterised and in use for electronics tests

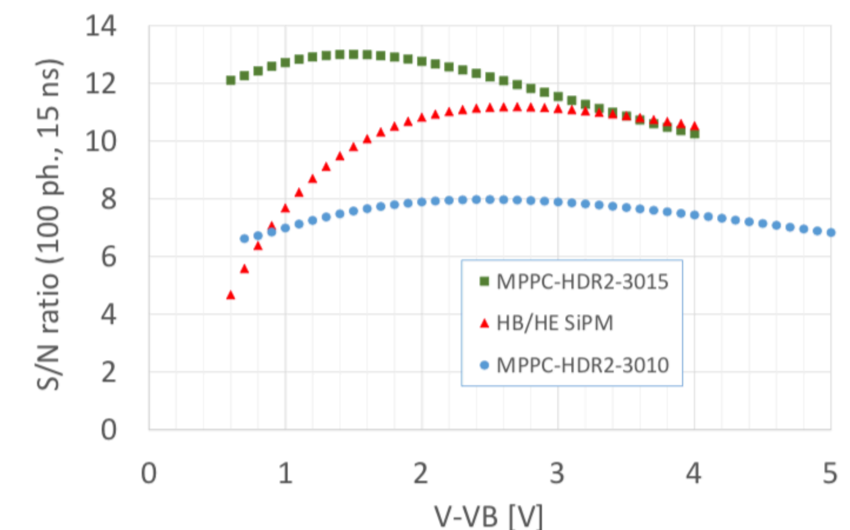
GHz noise levels at end of life

stay clear of PDE degradation by occupancy









Scintillator Module Assembly

First Tileboard prototype TB-1 produced

holds SiPMs, HGCROC2-SiPM, GBT-SCA (control), FEAST (DCDC), LEDs

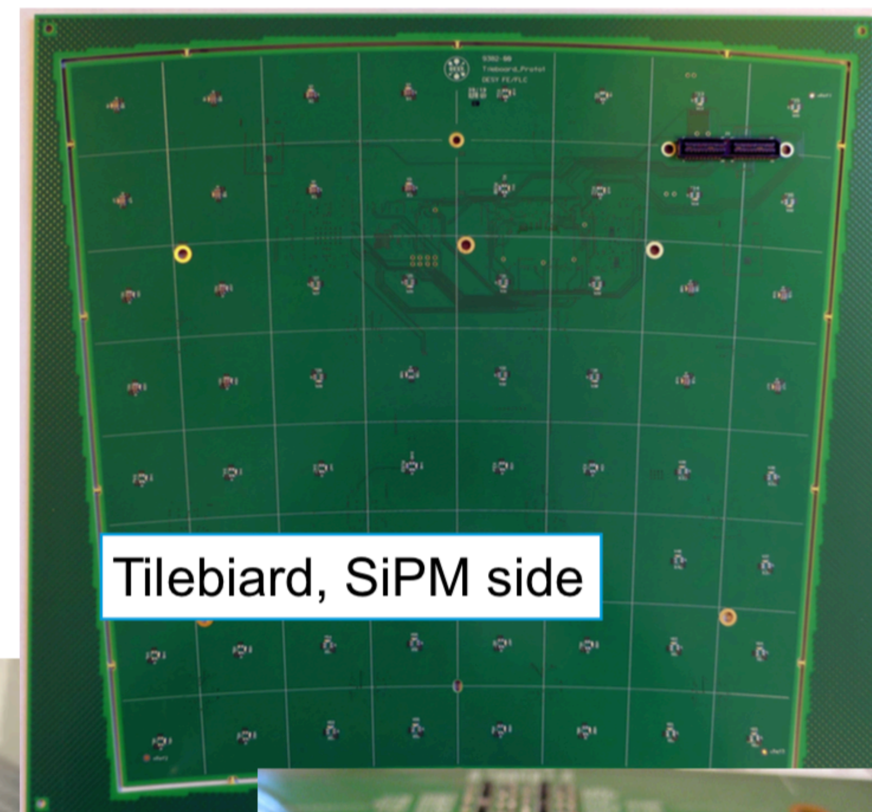
complex layout due to fine-pitch (0.6mm) HGCROC BGA

alive and sending data

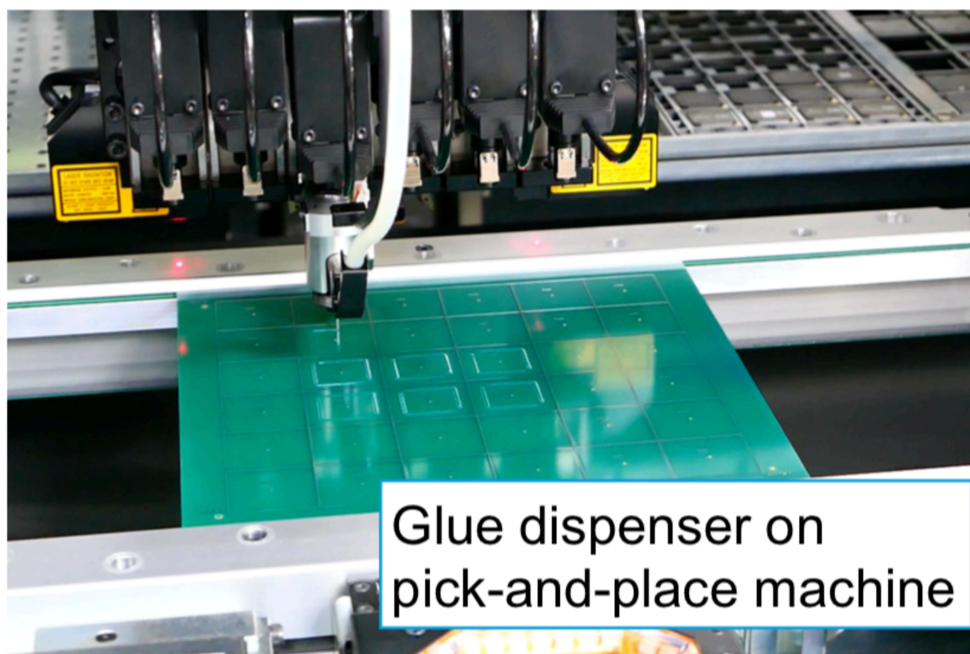
Assembly procedures for 4000 boards

building on CALICE experience

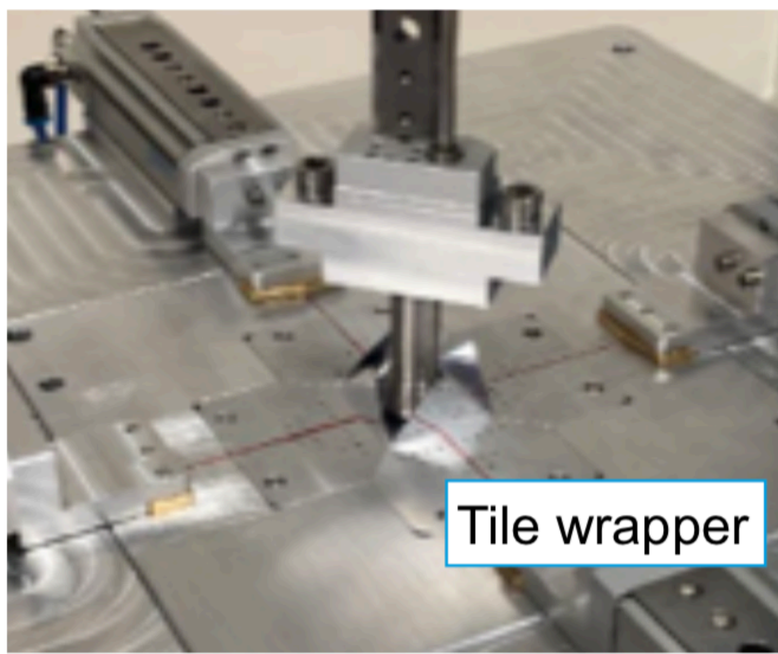
new techniques for foil cutting and tile glueing



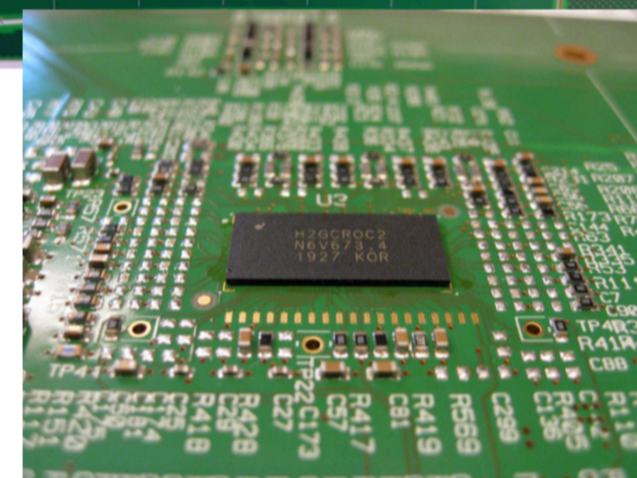
Tilebiard, SiPM side



Glue dispenser on pick-and-place machine



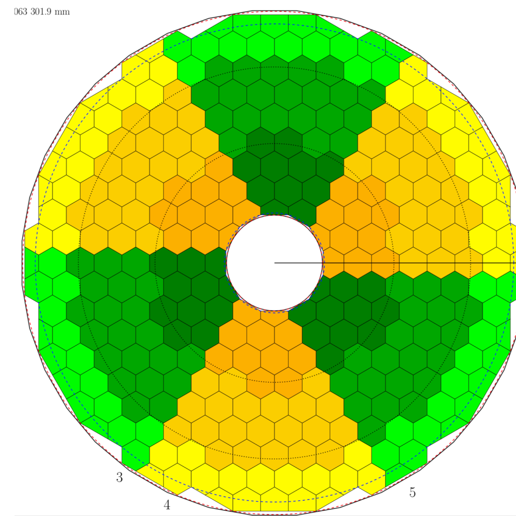
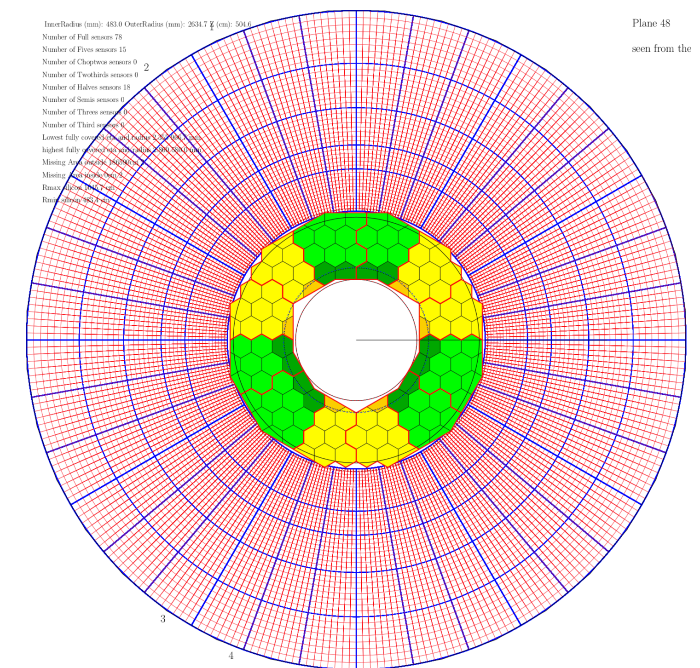
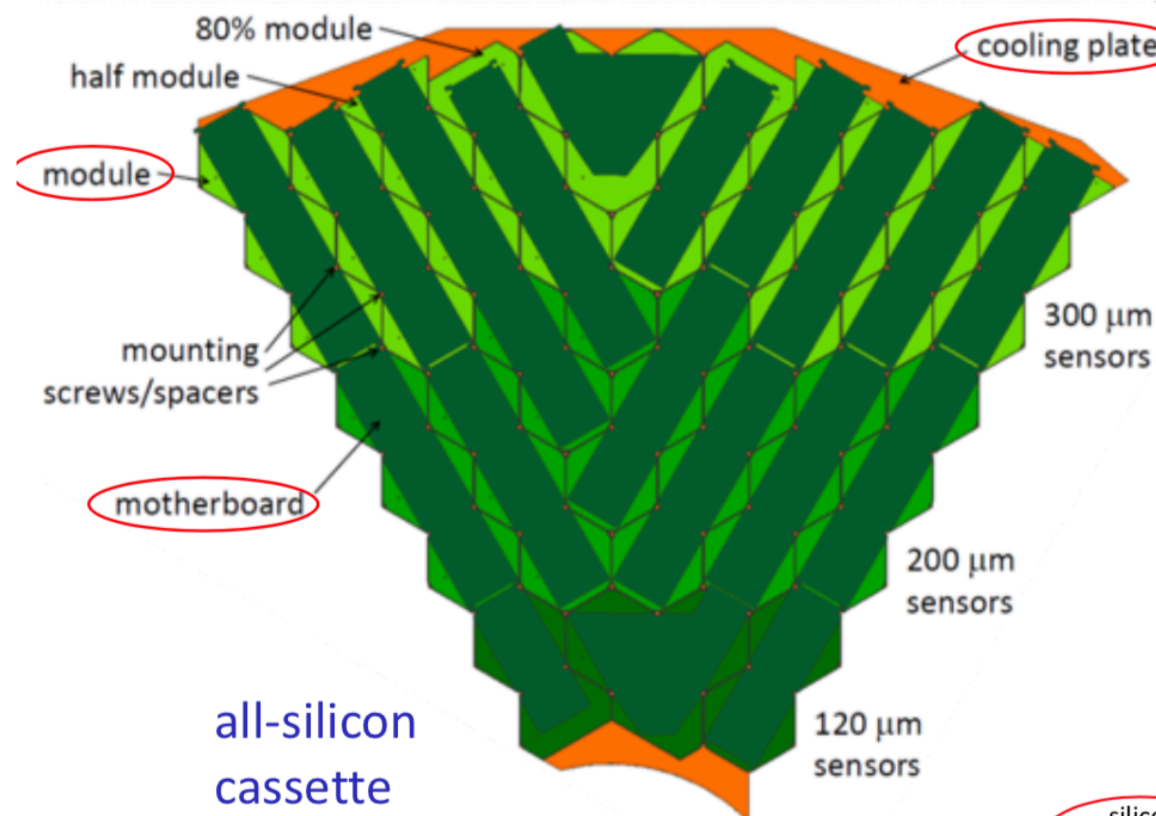
Tile wrapper

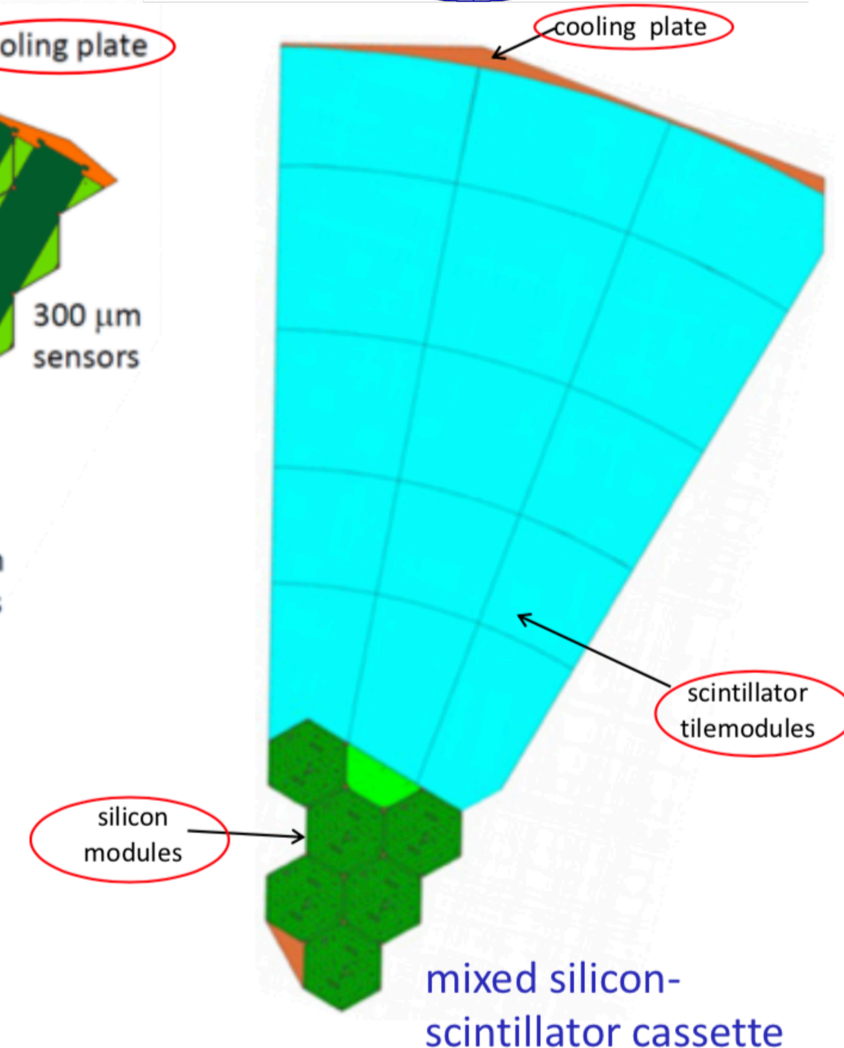


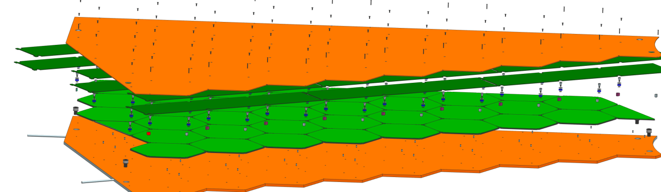
HGCROC-SiPM

Lateral Structure, Cassettes

- **Silicon and scintillator modules assembled into cassettes**
- **Supported and cooled by copper cooling plate**
- **Data from modules collected by motherboards**
- **Cassettes house all services and DC2DC converters**

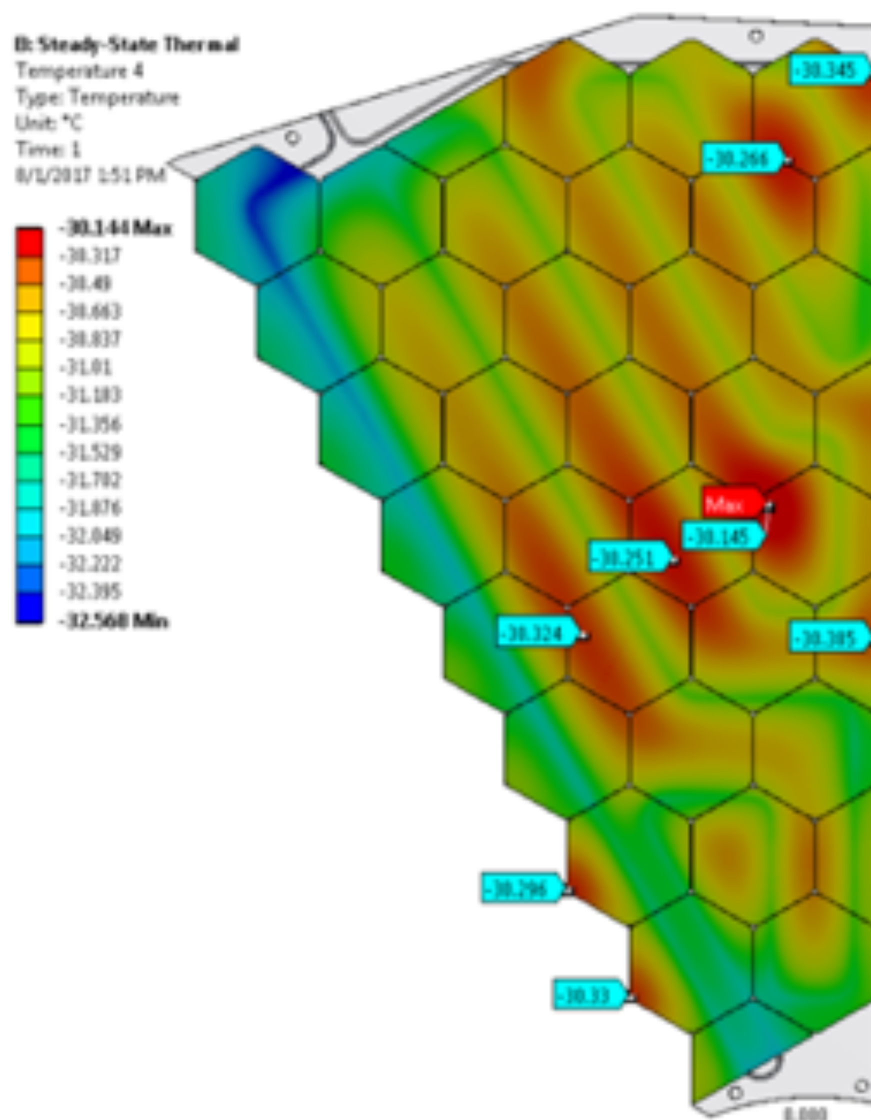




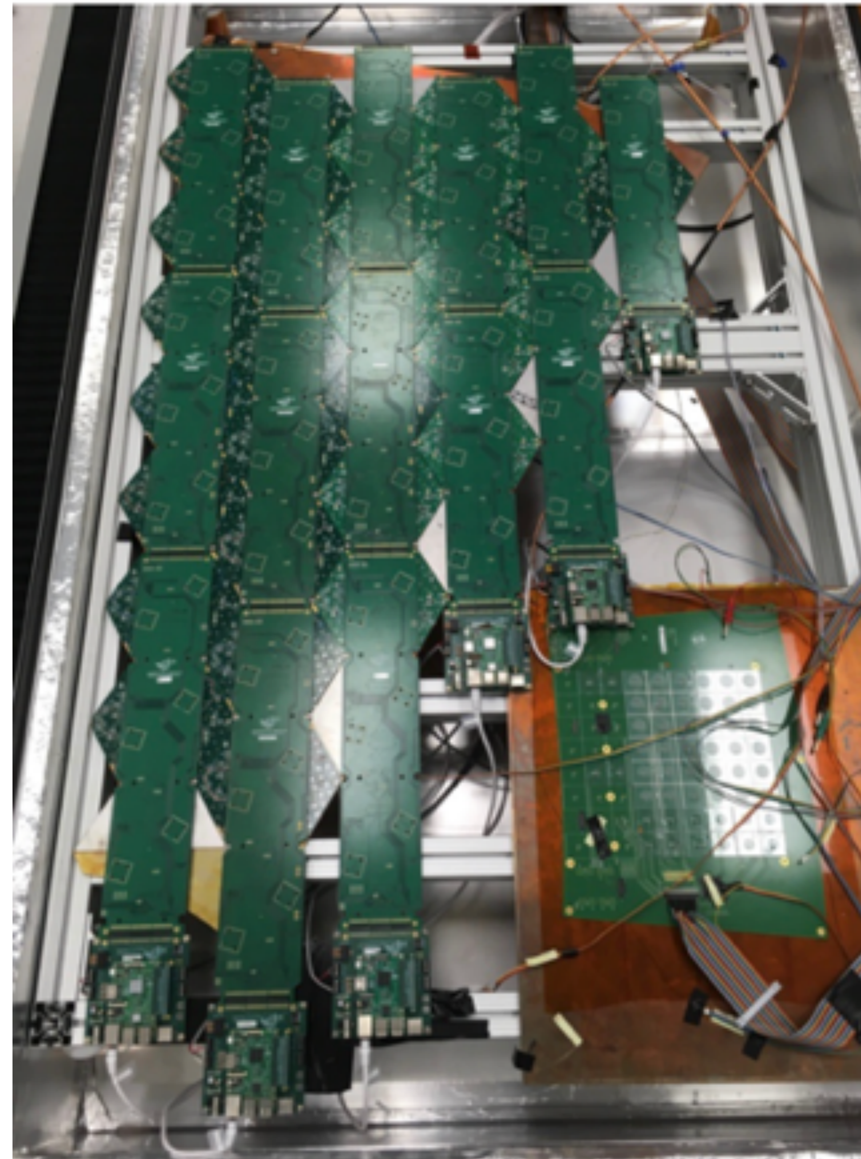


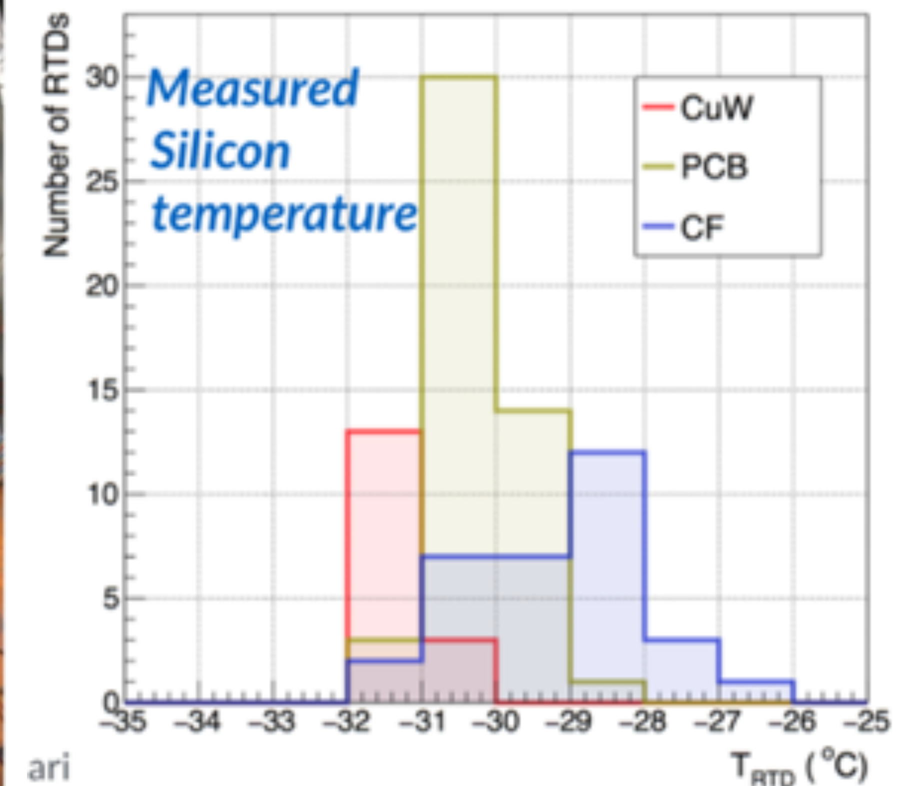


Cooling Performance

- **A mockup cassette has been fabricated to verify cooling performance**
- **With CO2 temperature at -35C and expected heatload of 270W, silicon sensors were maintained at -30C**







Front-End Electronics

Overall chip divided in two symmetrical parts

- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC: peak measurement, 10 bits @ 40 MHz
  - TDC: TOT (Time over Threshold), 12 bits (LSB = 50ps)
- Time
  - TDC: TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

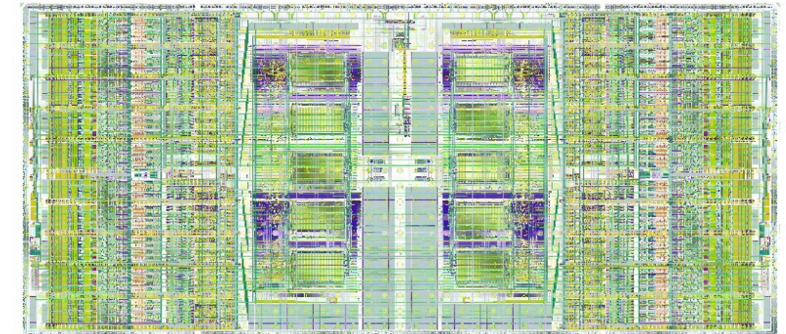
- DAQ path
  - 512 depth DRAM, circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1,28 GBPS links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1,28 GBPS links

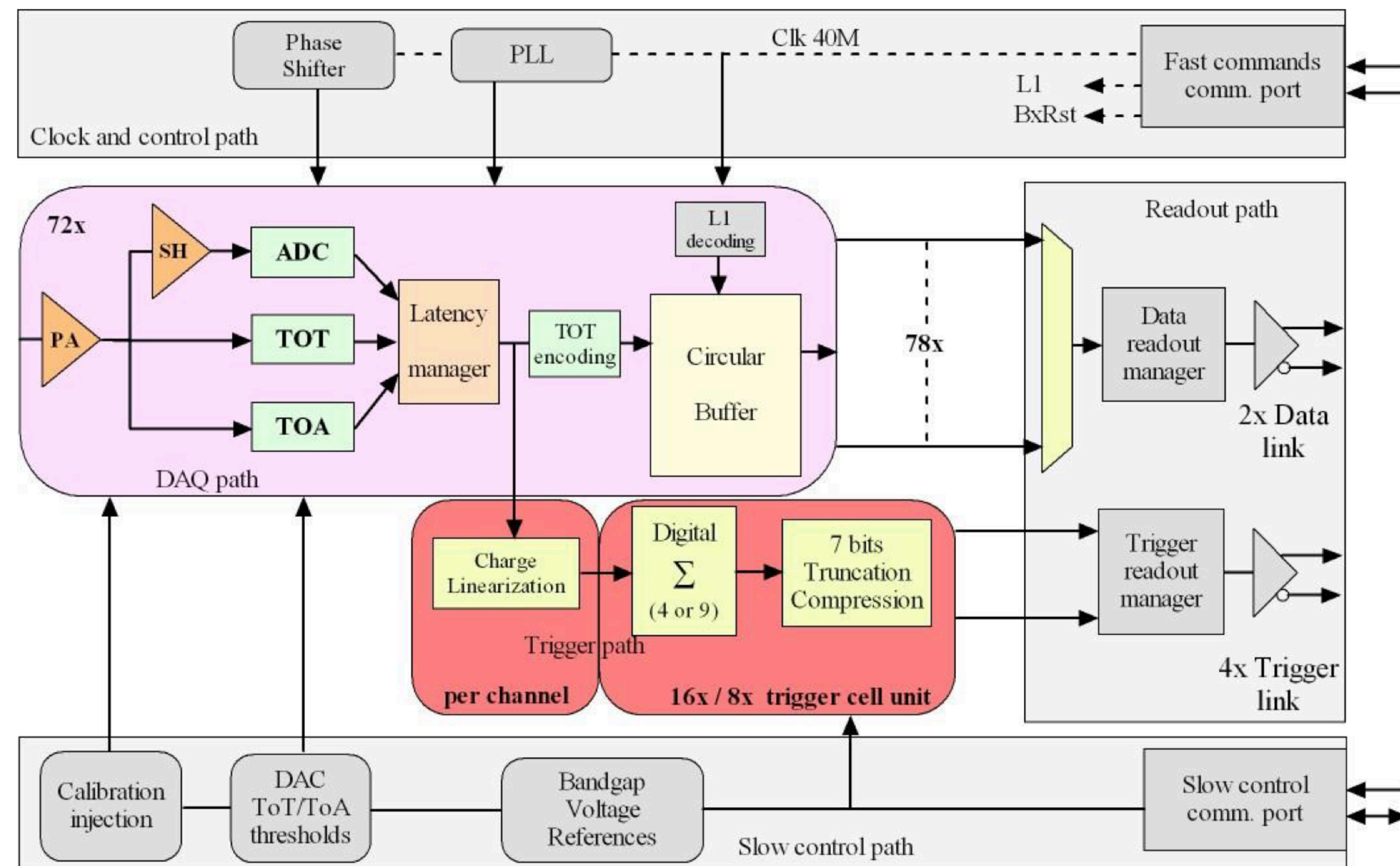
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

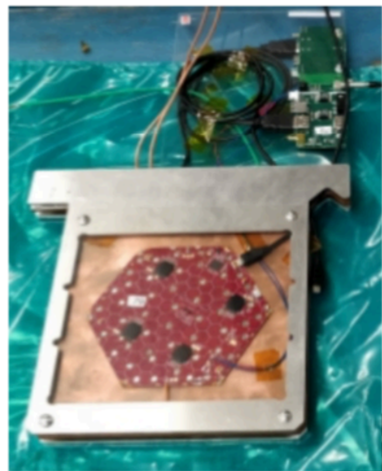
Ancillary blocks

- Bandgap
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL
- Adjustable phase for mixed domain

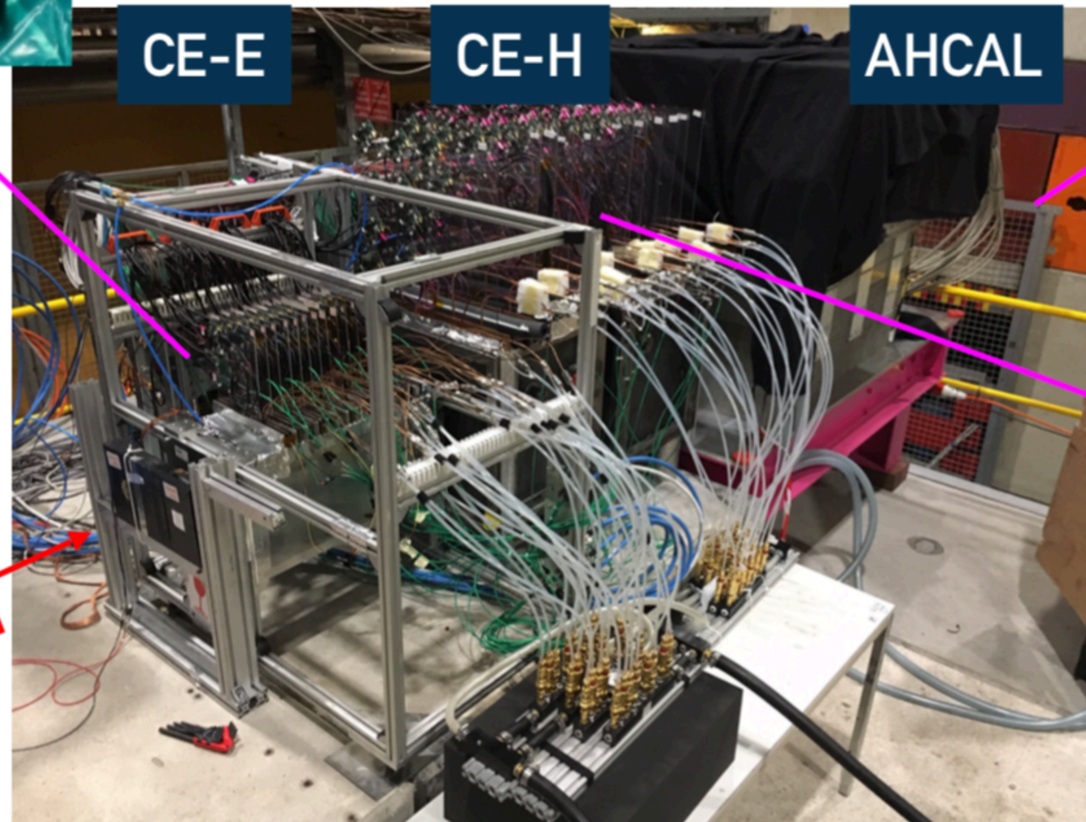


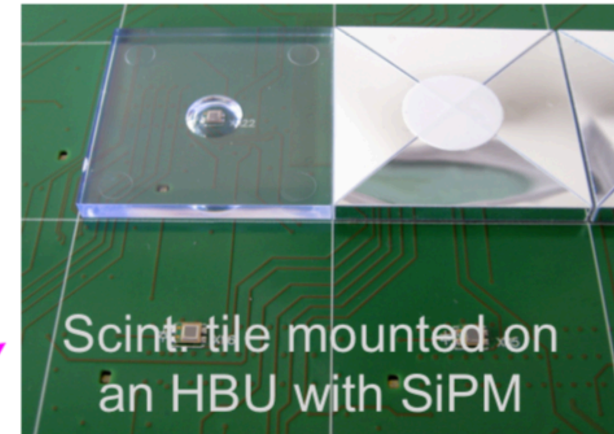


Beam Test Setup

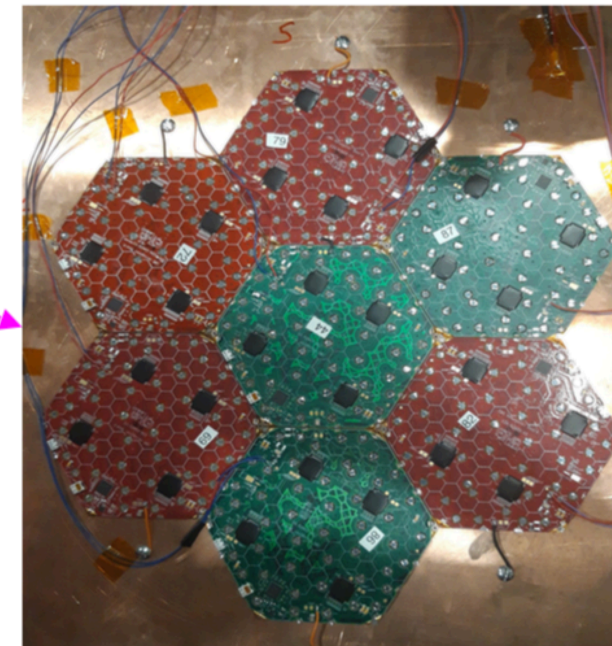


CE-E: Hanging file structure
- Double sided cassettes
- **Lead/Copper absorber**
- **~ 26 X_0, 1.4 λ_{int}**





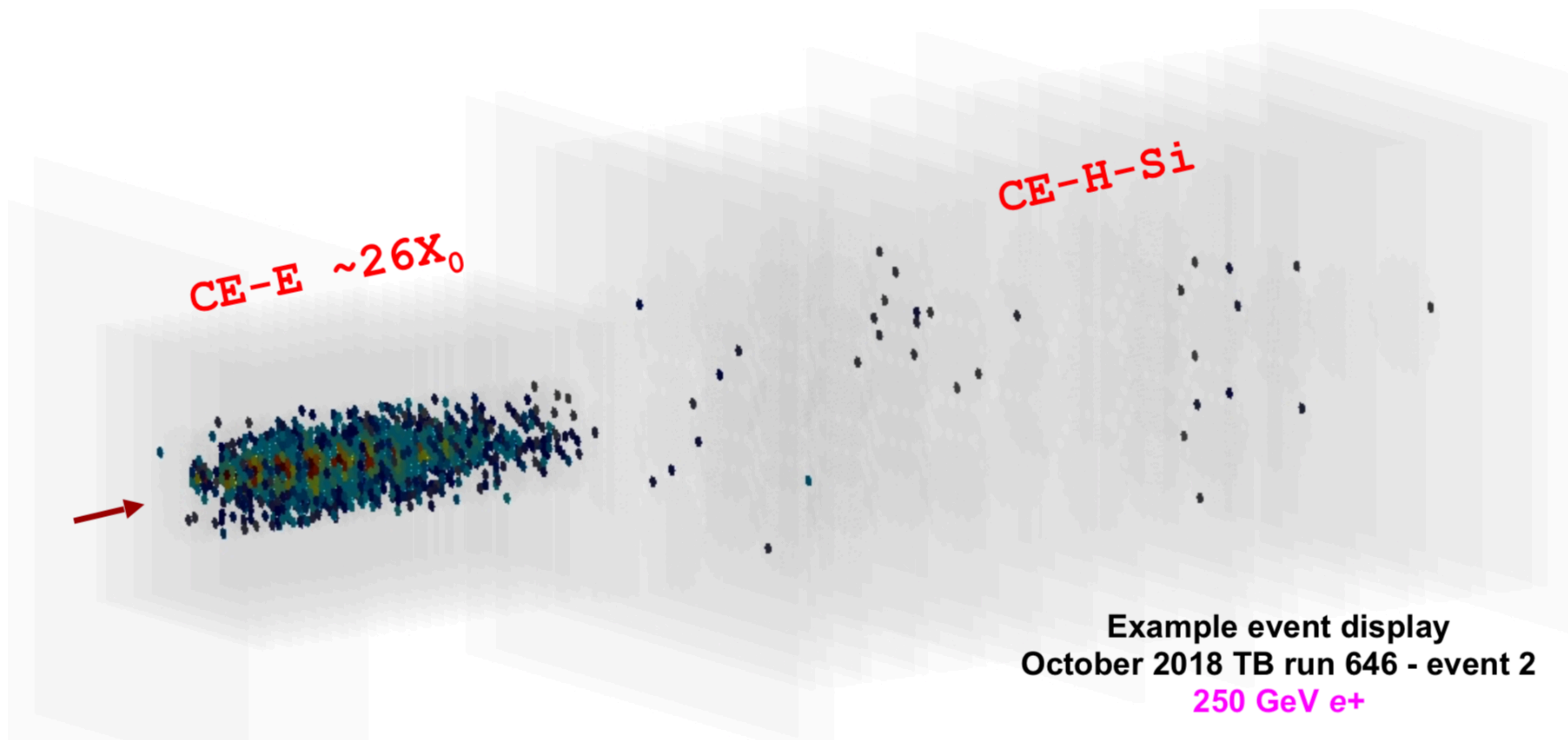
CALICE AHCAL:
- Scintillator/SiPM
- **Steel absorber**
- 39 layers, 14k channels
- **~ 4.4 λ_{int}**



CE-H: Hanging file structure
- Single sided cassettes
- **Steel absorber**
- **~ 3.4 λ_{int}**

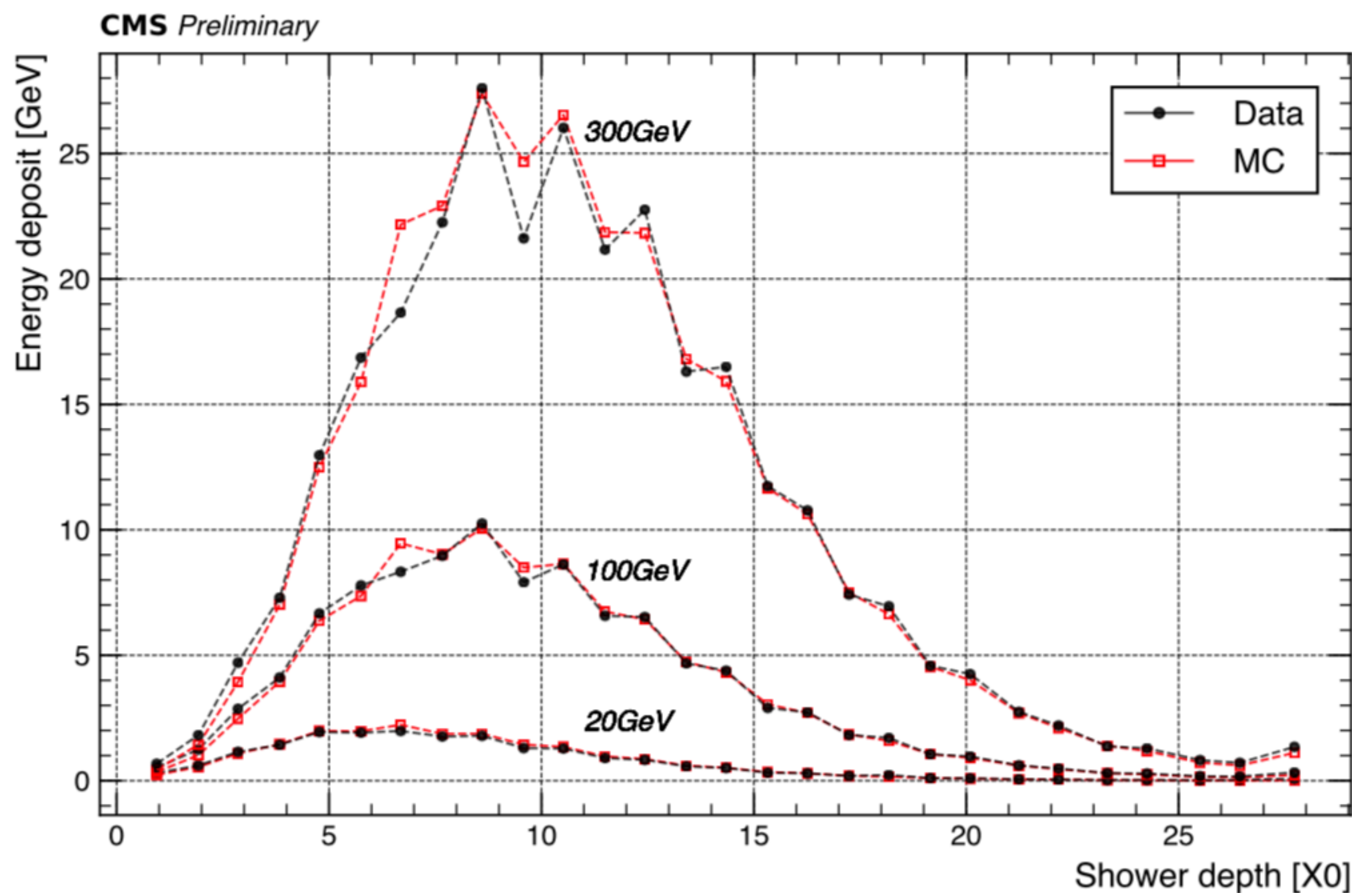
First large-scale test of more than 90 HGCAL modules in October 2018 data-taking at CERN.
The setup was exposed to e^+ & π beam of energies ranging from 20 to 300 GeV and 200 GeV μ beams.

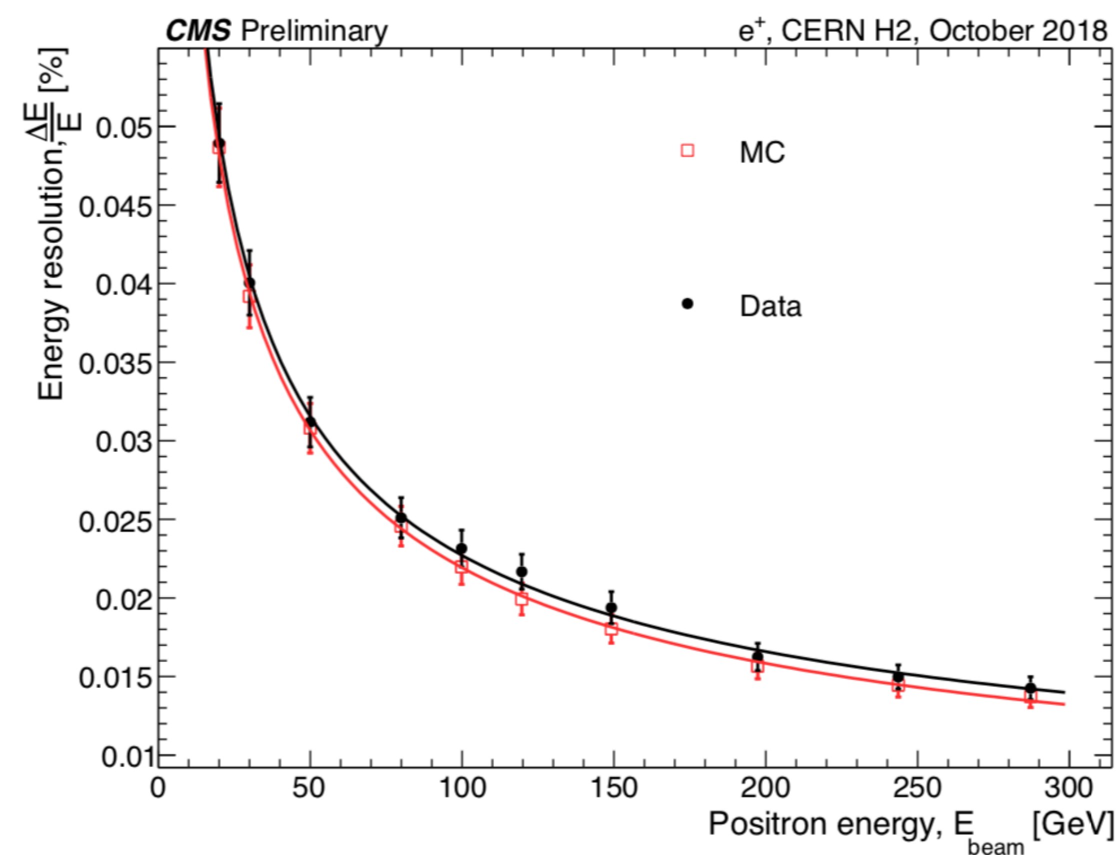
Example Event Display

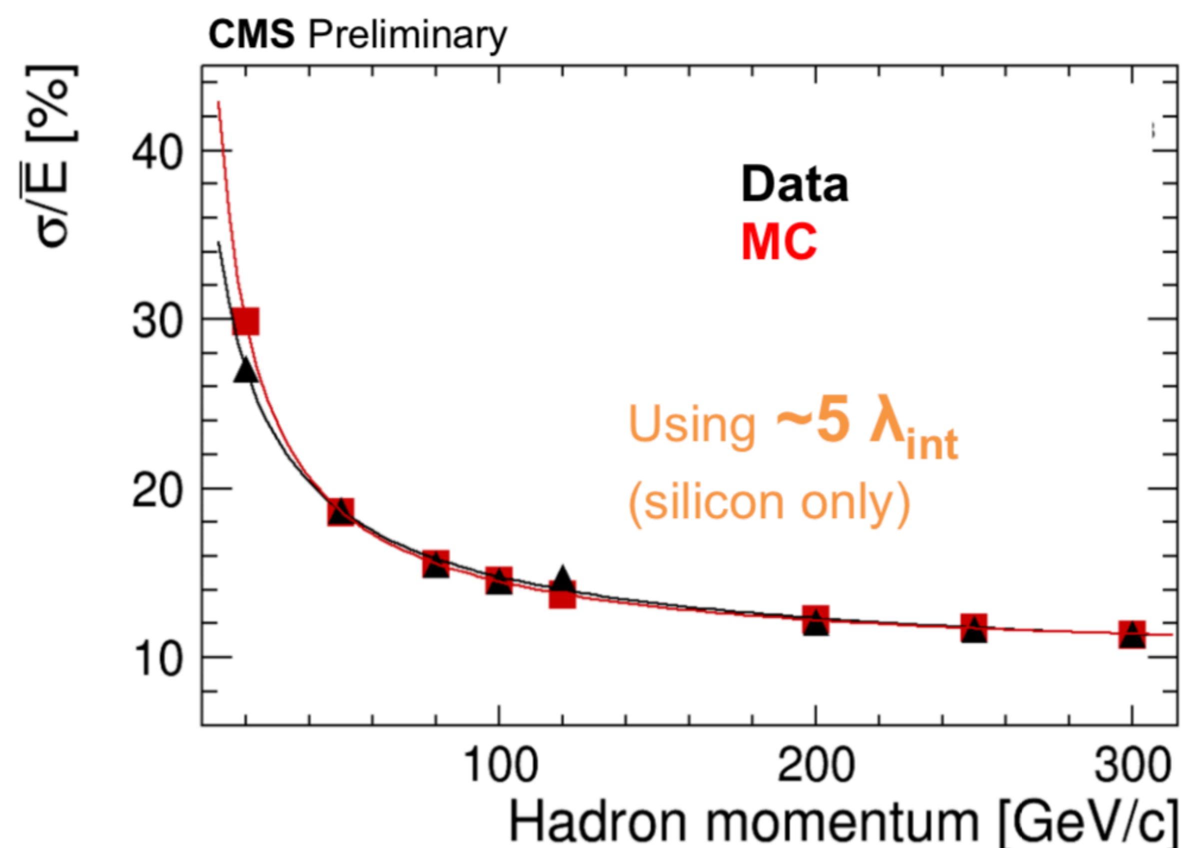


Performance

Longitudinal shower profile: average energy deposited by e+ showers in each layer of CE-E

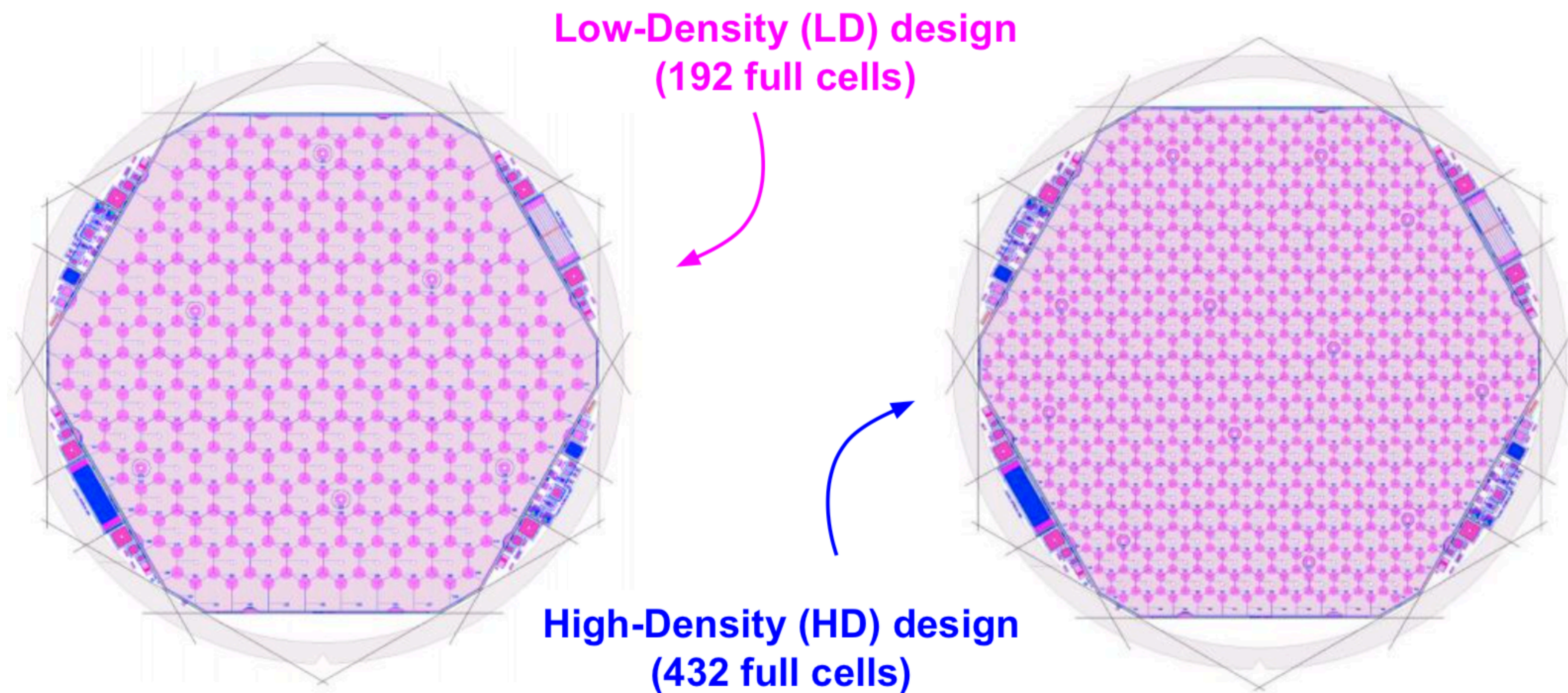




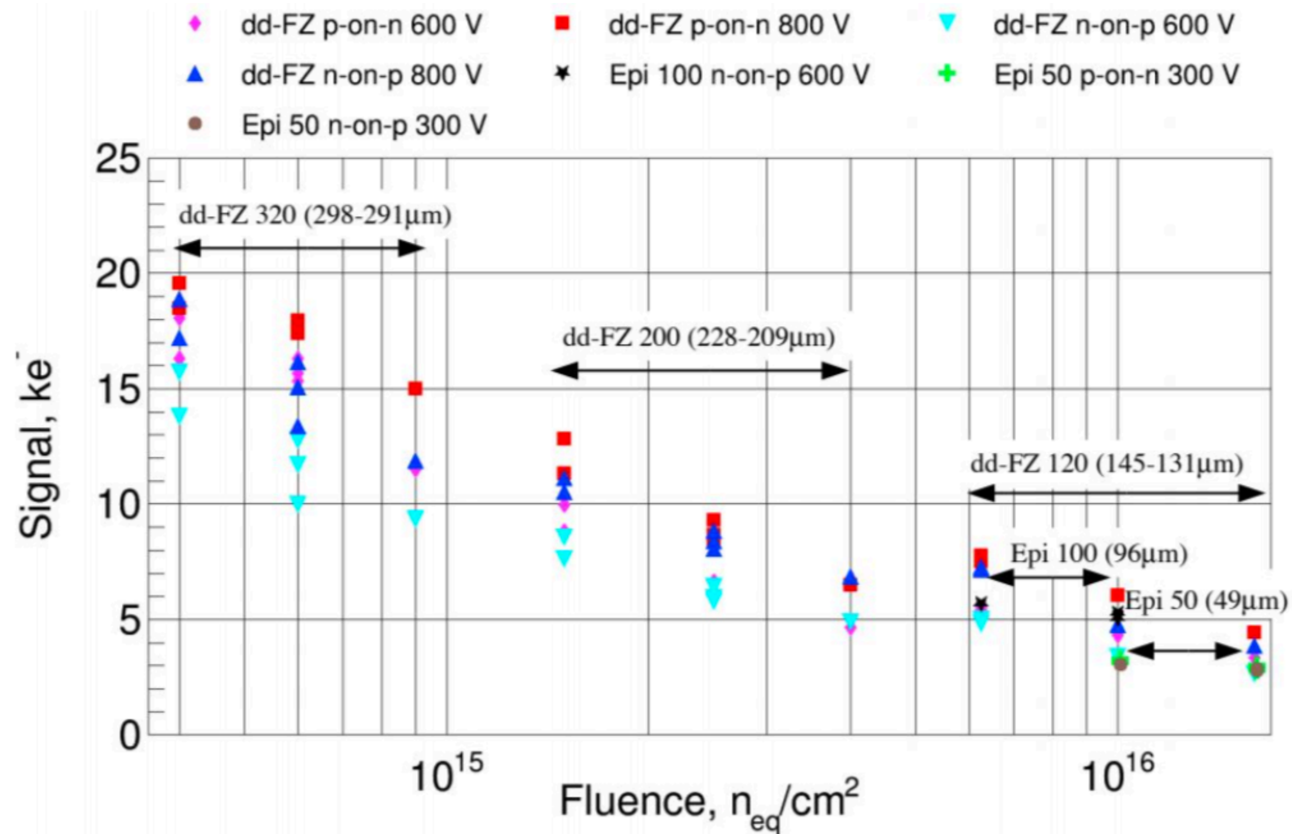


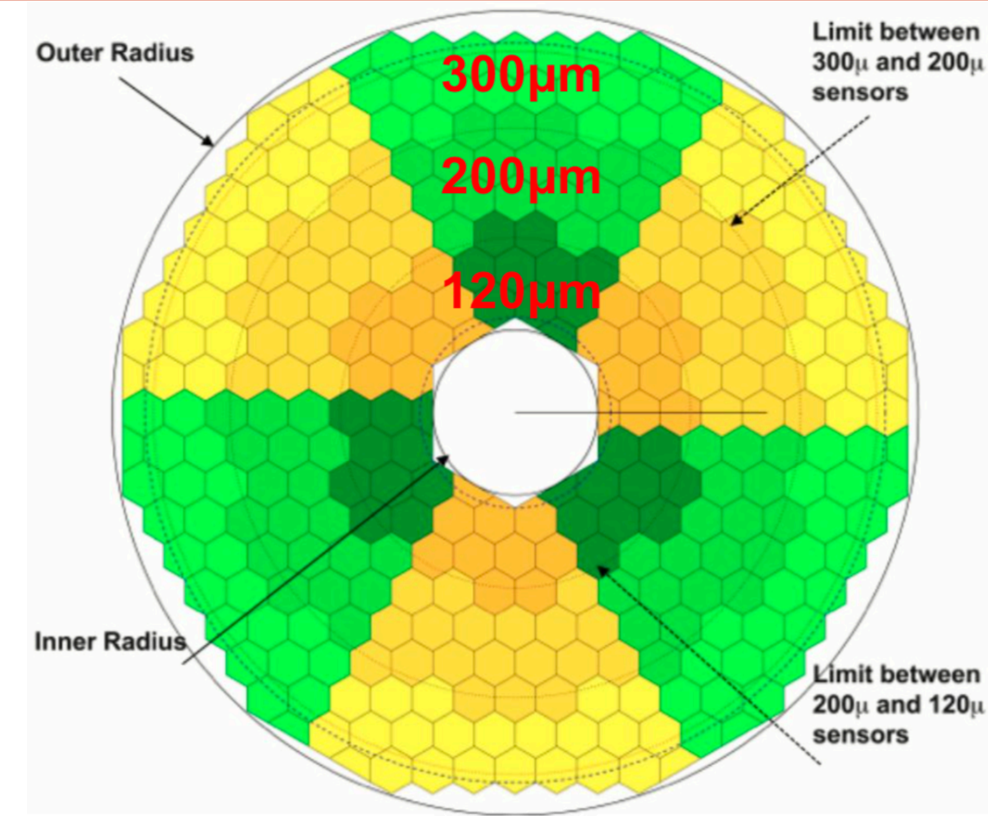
- The GEANT4 FTFP_BERT_EMN physics list closely models the longitudinal shower shapes and energy resolution measured in the data using e+ and pion momenta raging from 20-300GeV

Silicon Sensor Characterization



Sensor Thickness and Radiation Hardness





6” 135-cells (LD)

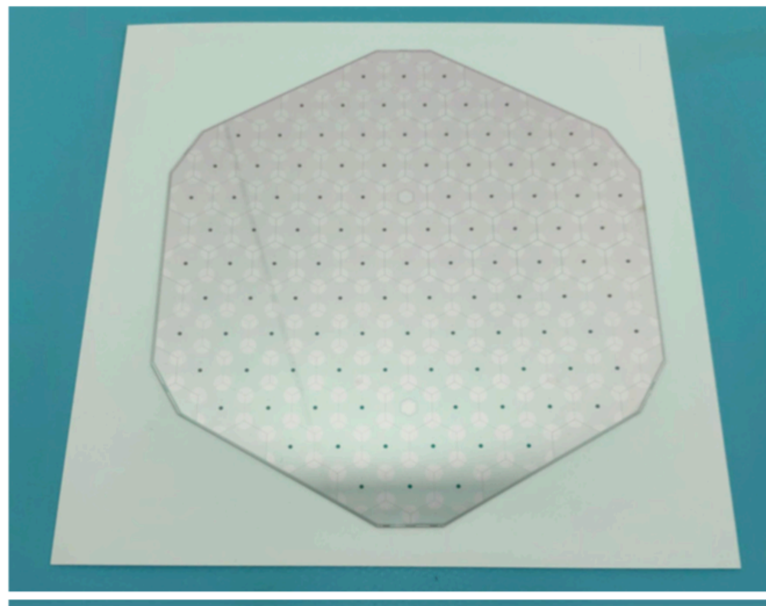
- standard-diffused FZ
- 300µm active thickness
- n- and p-type (individual and common)

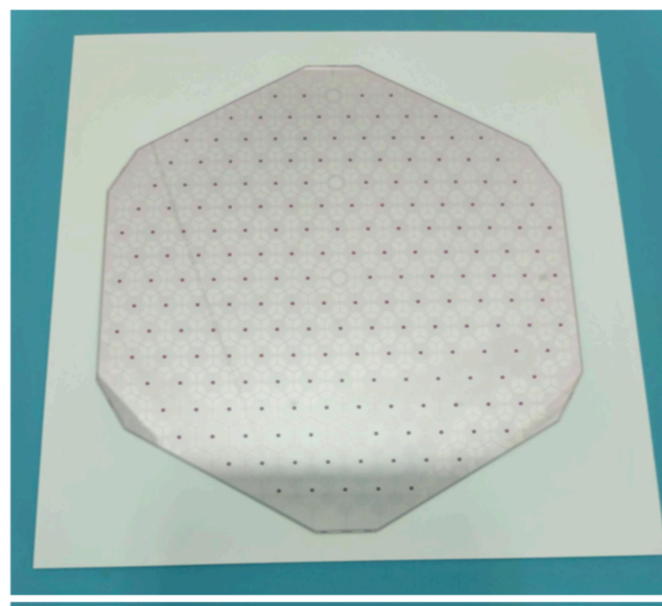
6” 239-cells (HD)

- deep-diffused FZ (+ jumper cells)
- 120µm active thickness
- n- and p-type (individual and common)

8” 192-cells (LD)

- shallow-diffused FZ (300µm & 200µm)
- epitaxial (120µm active thickness)
- p-type (individual and common)

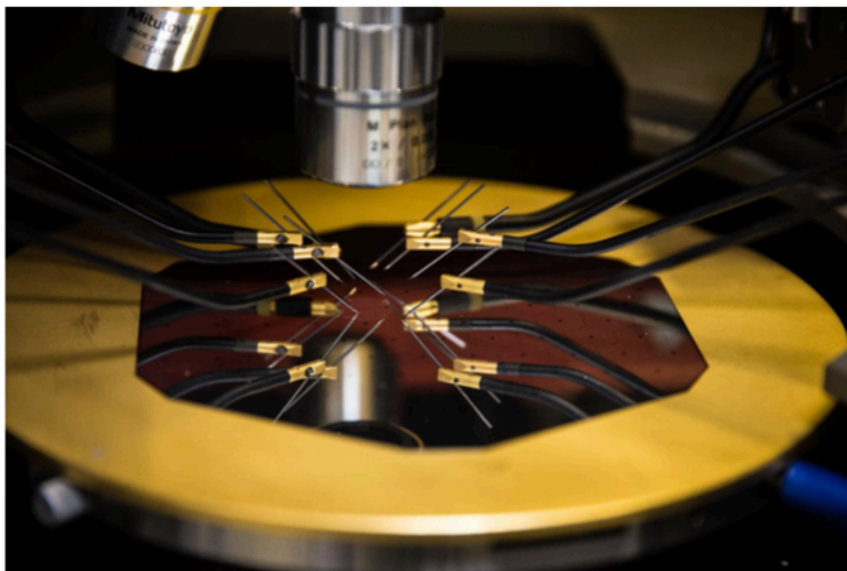


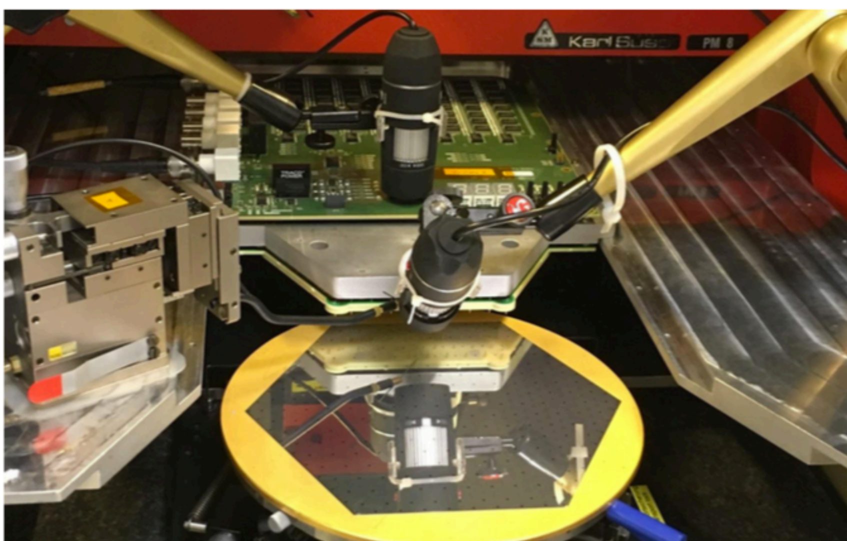


Versatyle Characterization Systems

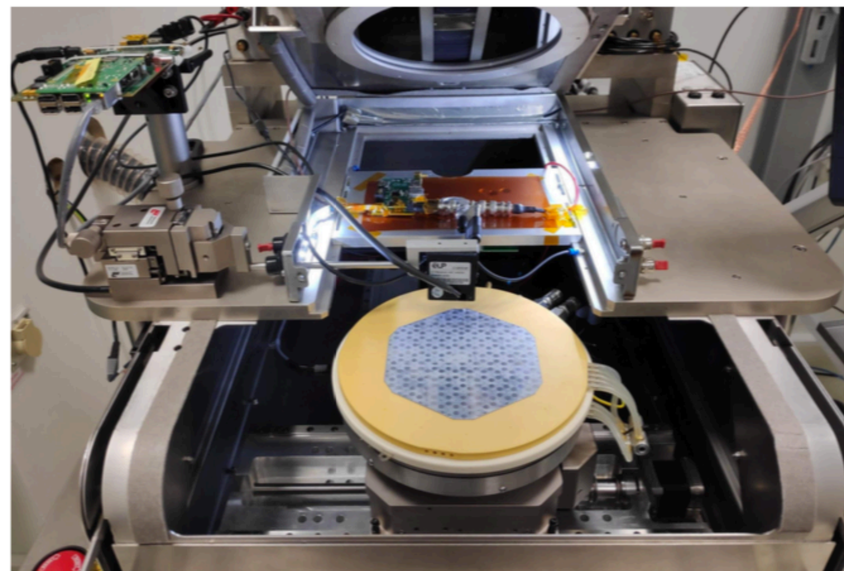
- **The sensor is DC coupled and no bias circuitry is present in the design**
- **Versatile systems developed for characterization of full wafer size silicon sensors**

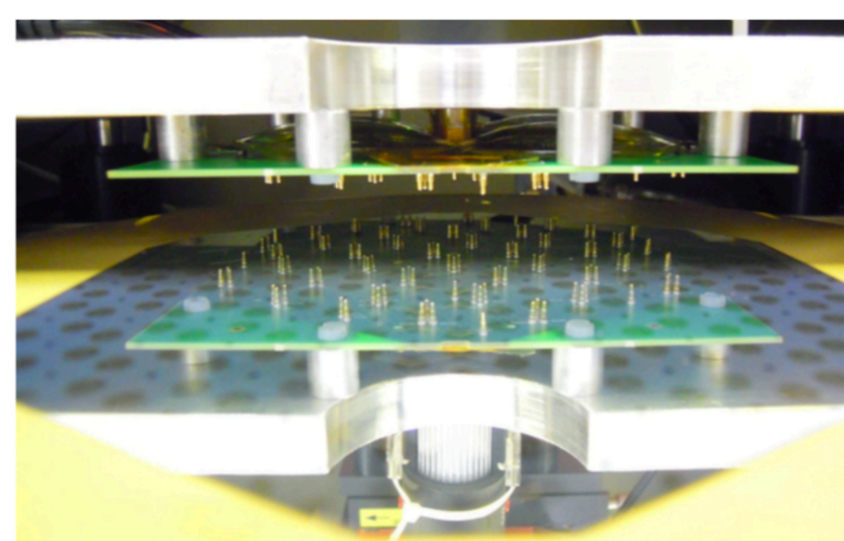
CV/IV



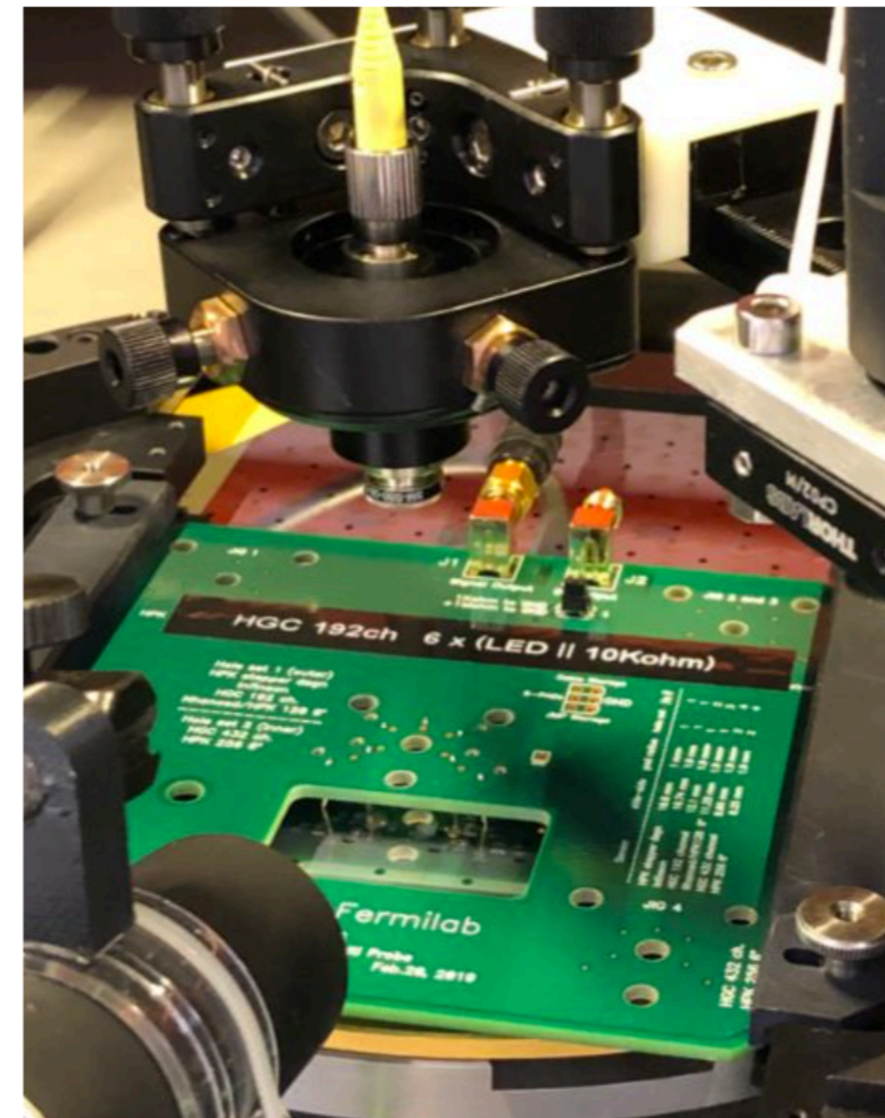


Noise





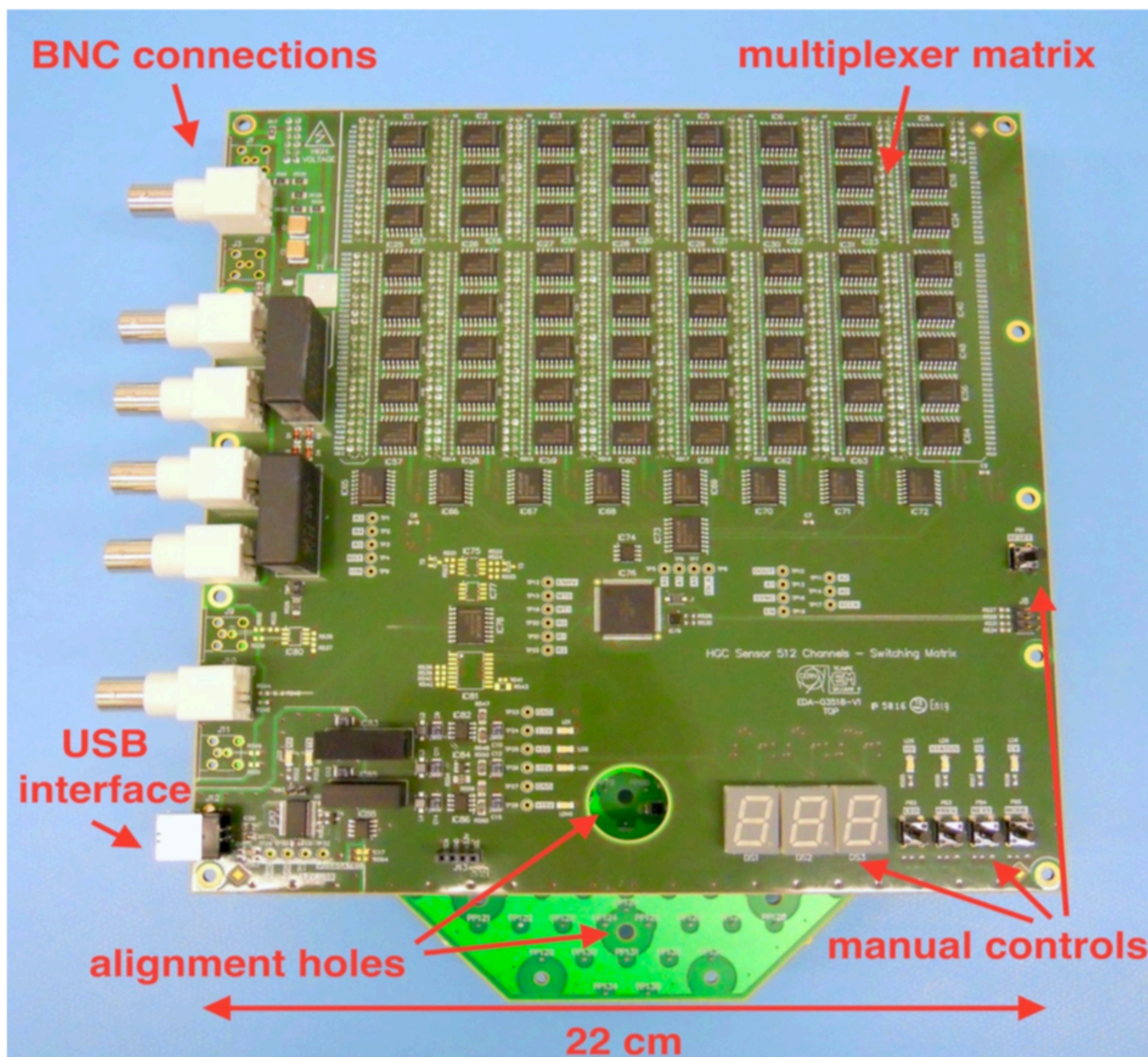
TCT



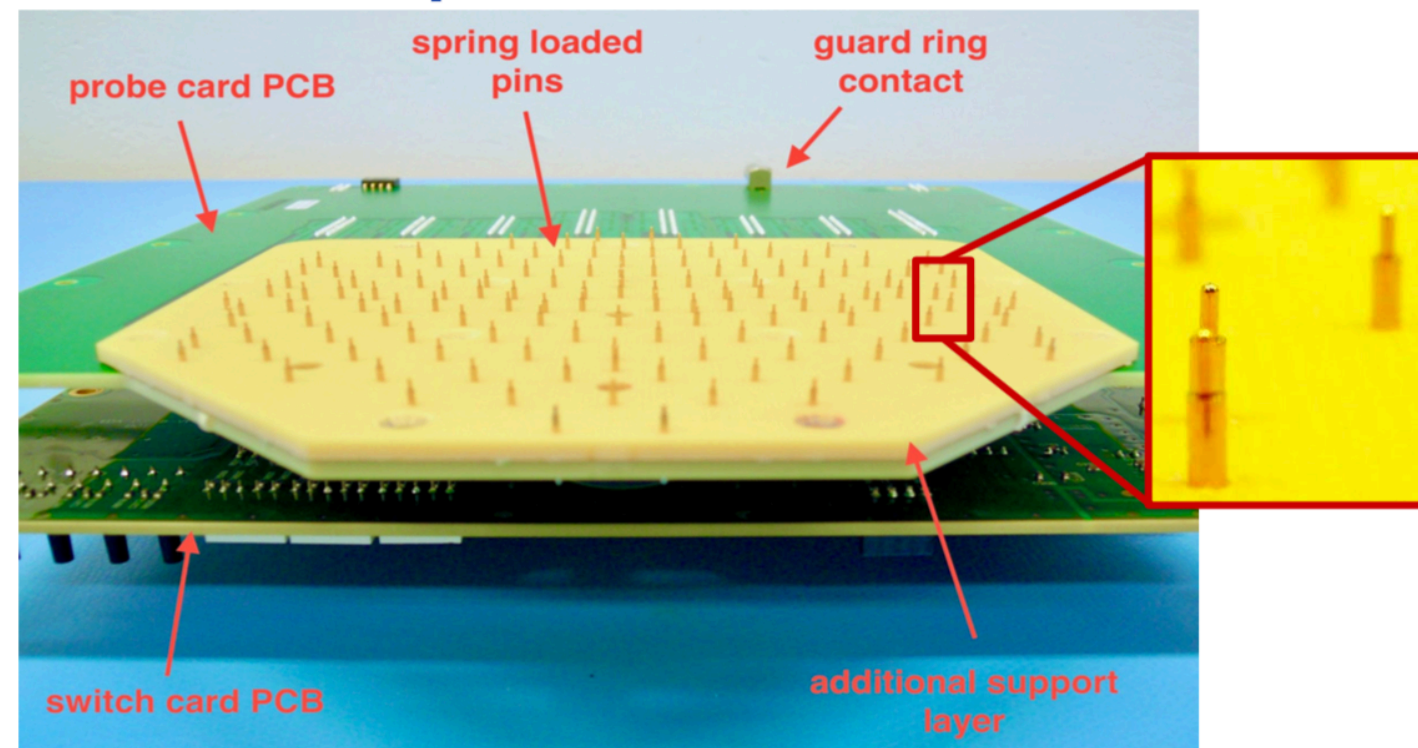
CV/IV - ARRAY (switching mAtRix pRobe cArd sYstem))

- **Dual card setup to automatically measure CV and IV of individual cells**
  - Switch card: contains all the active components and electronics
  - Probe card: routes the switchcard's channels to the sensors' cells using spring loaded pins

switch card



probe card



E. Pitters, NIMA 940 (2019) 168–173

Capacitance Measurements

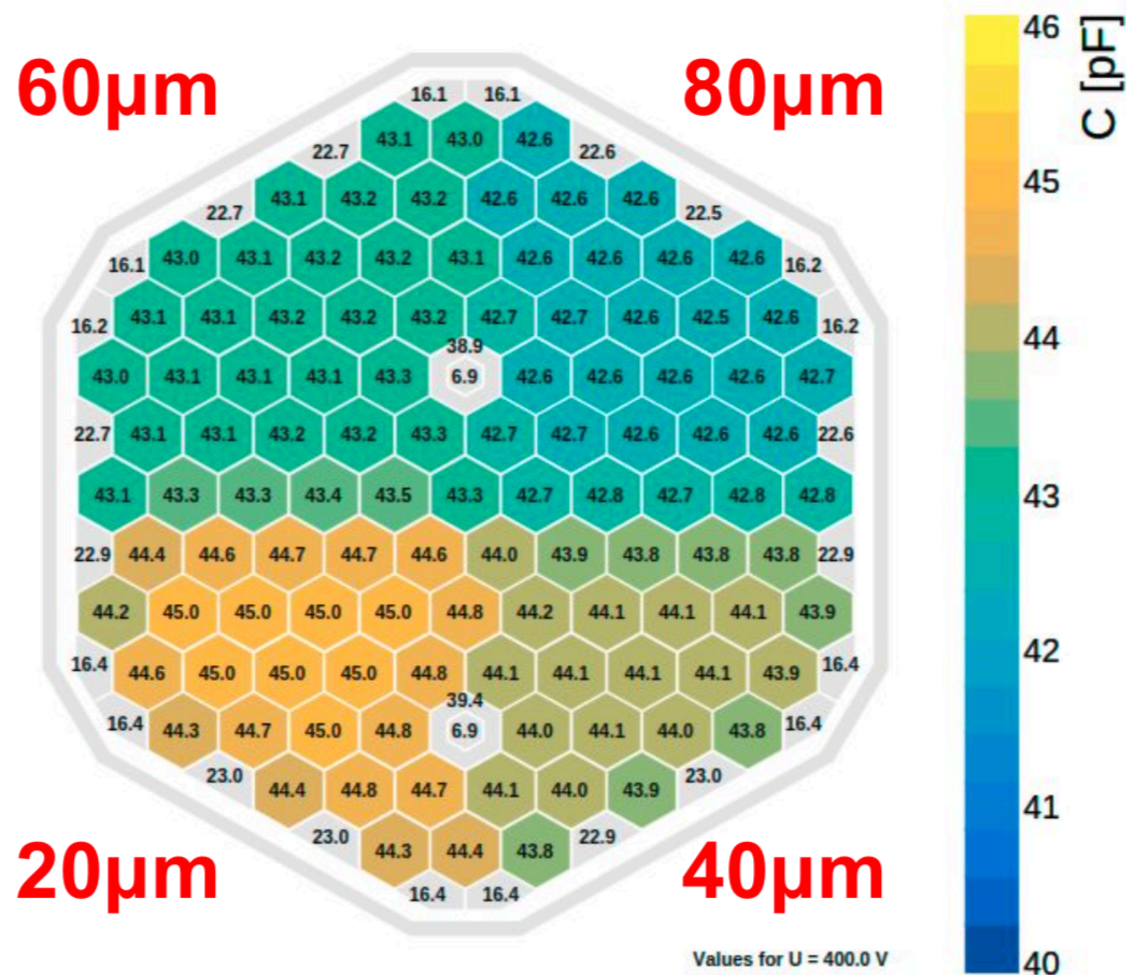
- **Capacitance measurements are corrected with open measurements**

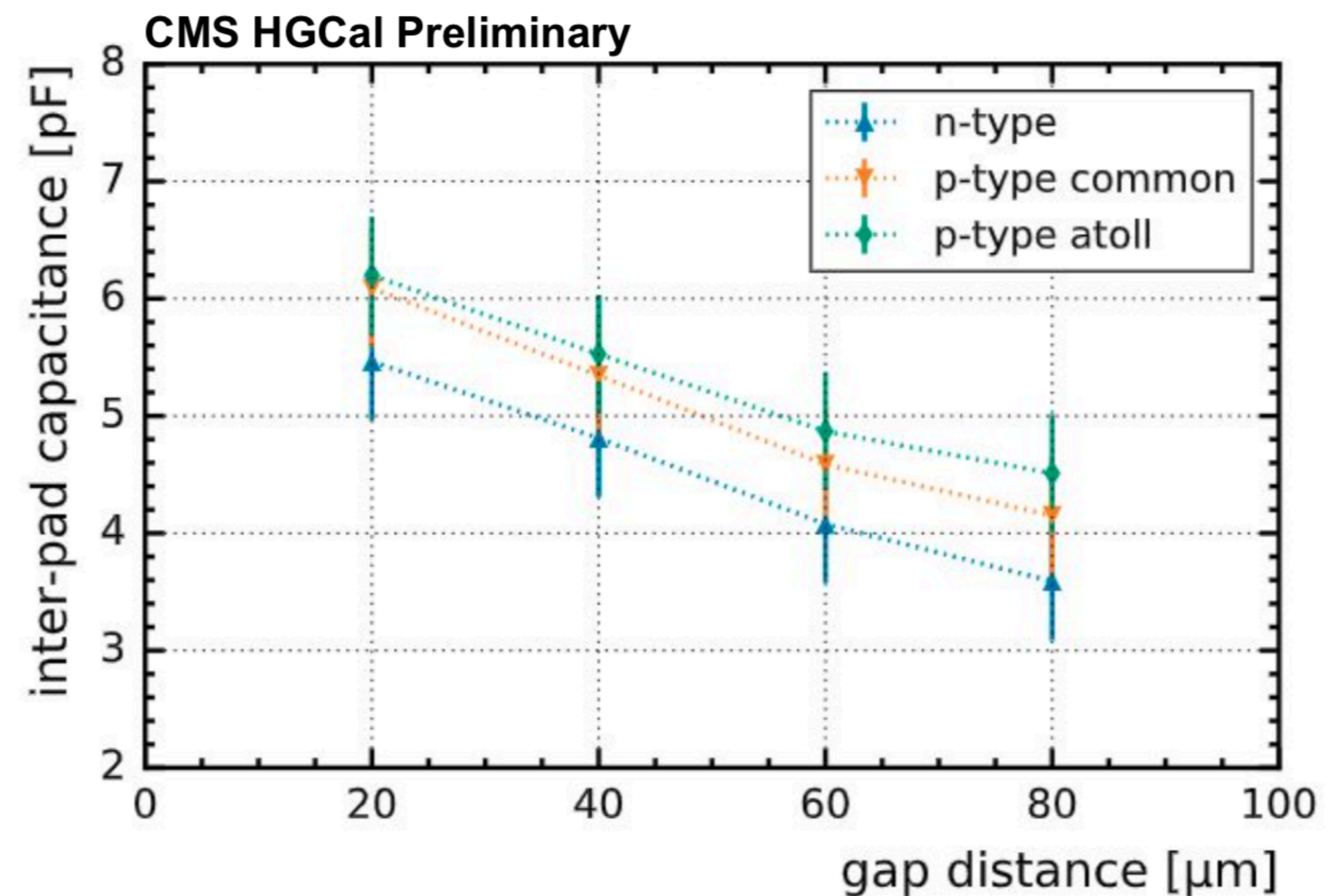
$$C_{corr} = C_{meas} - C_{open}$$

- **Sensitive to inter-pad capacitance:**

$$C_{inter} = C_{corr} - C_{bulk} \text{ where } C_{bulk} \sim \varepsilon_0 \varepsilon_r A / d$$

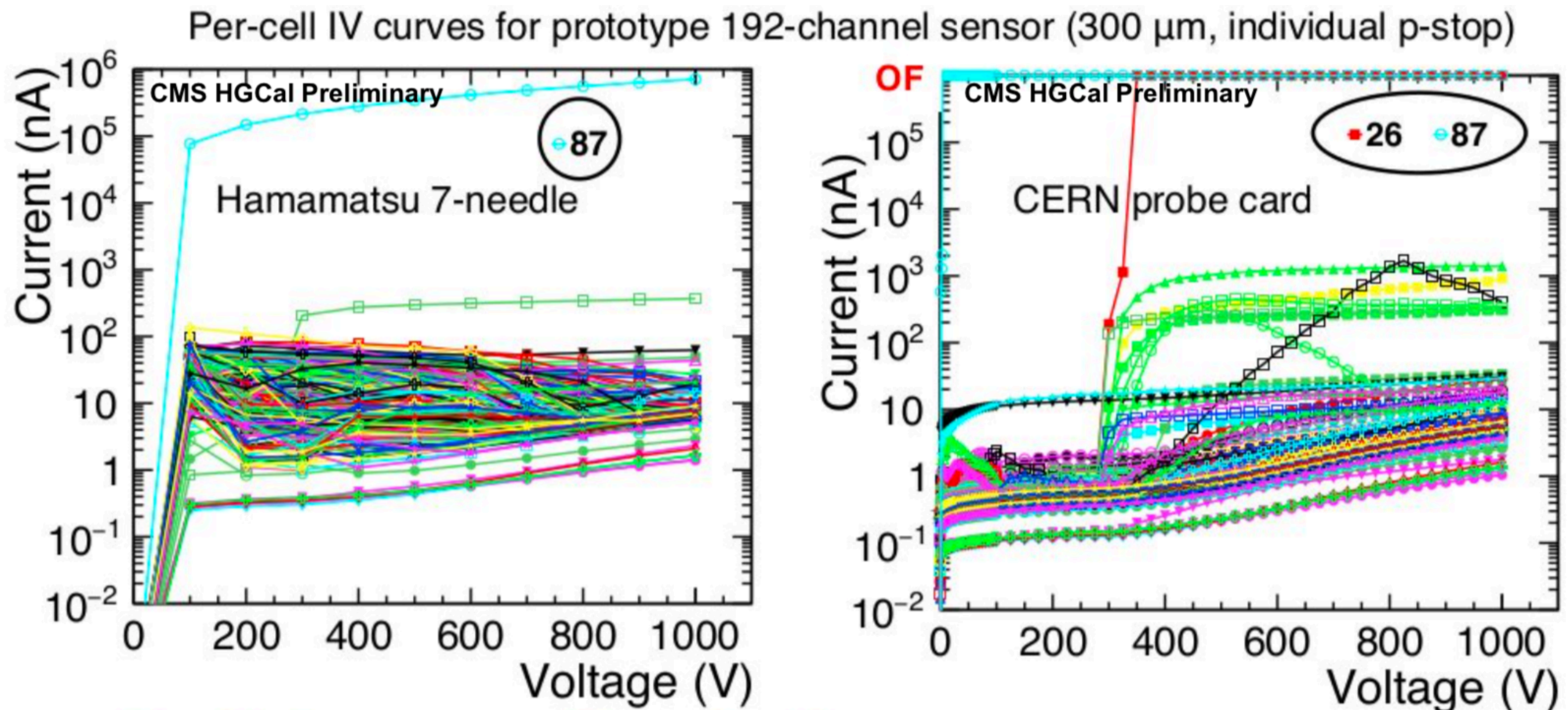
- **6” sensors with varying gap size between pads**





Leakage Current Measurements

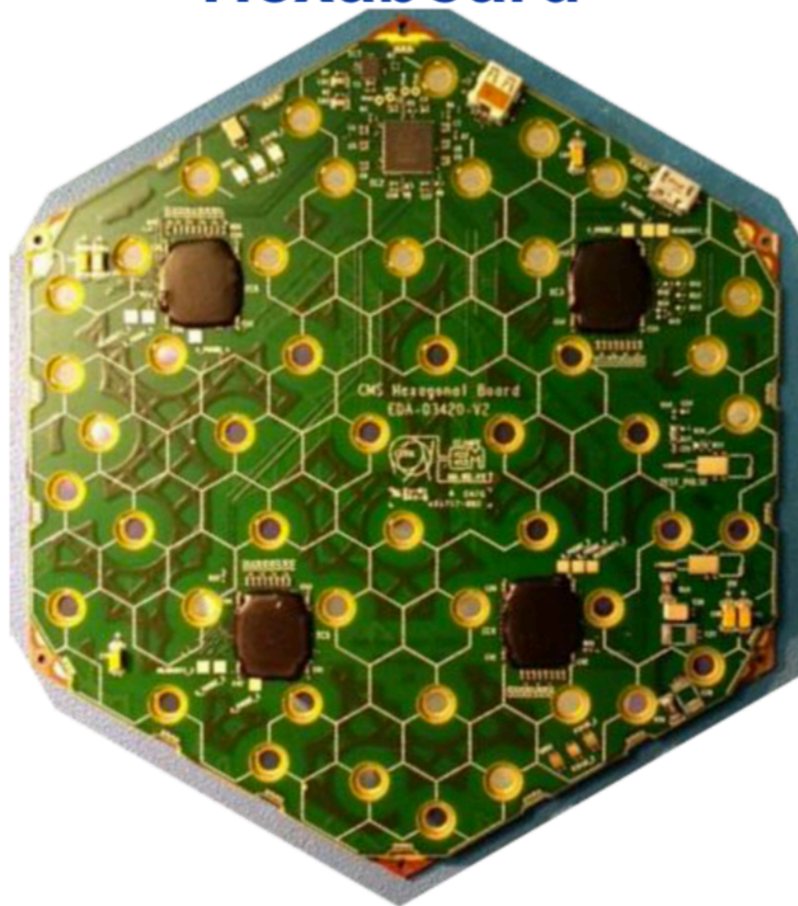
- **8" sensor types: epi 120um and shallow-diffused FZ 200/300um**
- **120um sensors have good quality: ~0.1uA at 1000V**
- **Backside fragility observed on 200/300um sensors**
  - Good agreement between HPK and probe card measurements



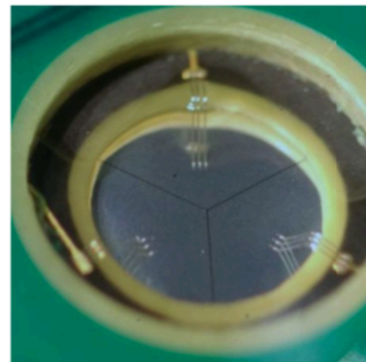
Hexaboard Probecard for Noise Measurements

- **Module readout PCB (Hexaboard) so far used in HGCAL beam test, adapted to a probe card**
  - Spring loaded pins used for contact instead of wire-bonds
  - Additional mechanical infrastructure for integration into sensor probe station
- **Allows noise testing of irradiated sensors**
  - without irradiating the readout board

Hexaboard

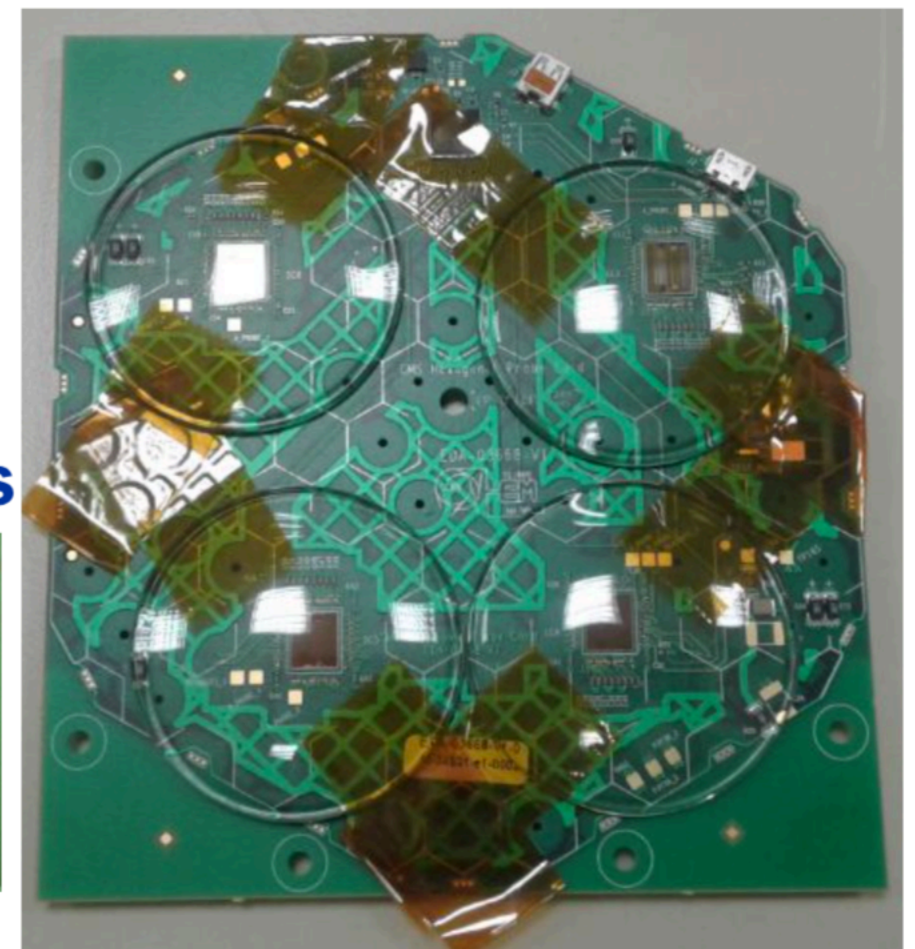


Wirebonds



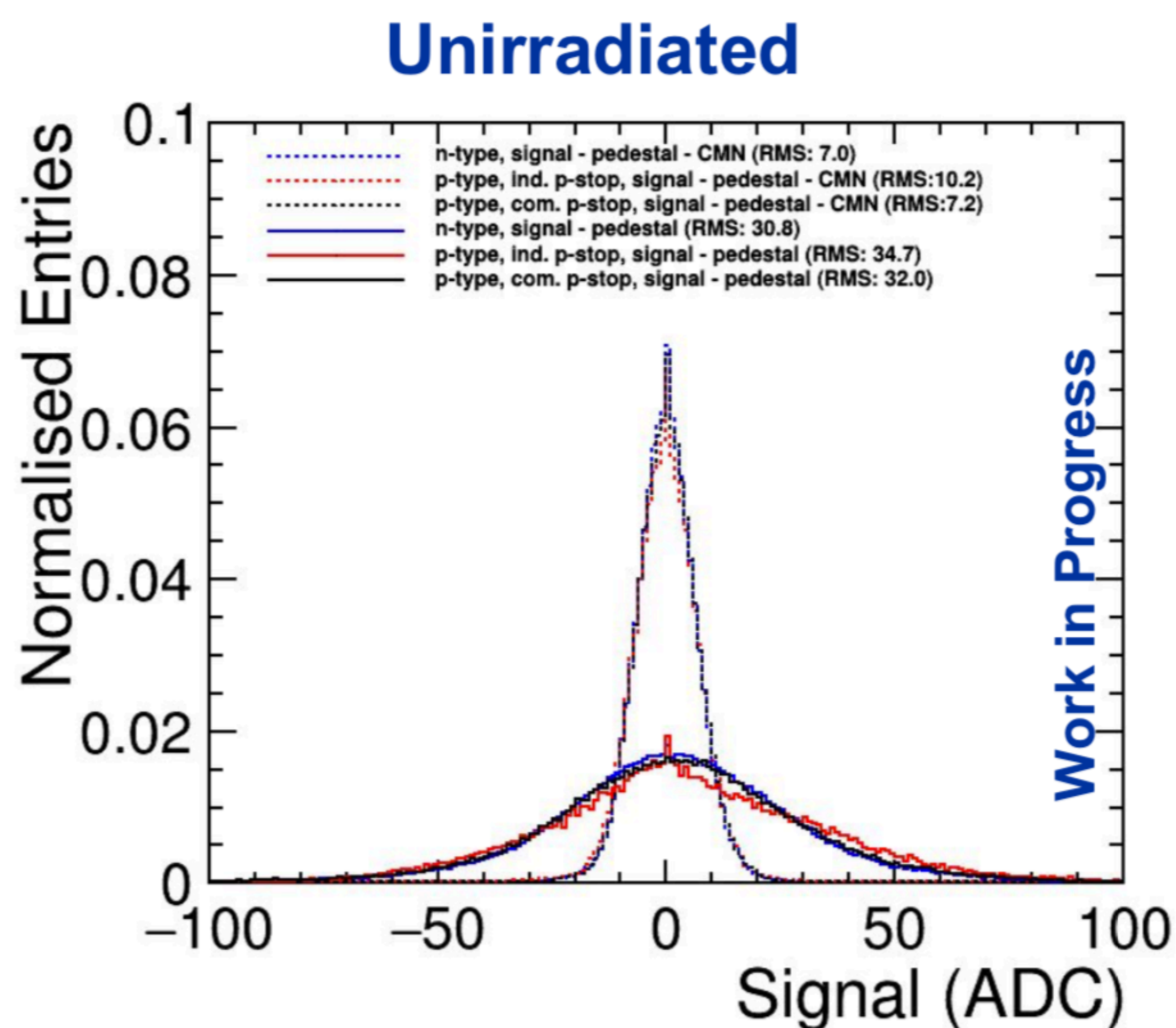
Pogo-pins

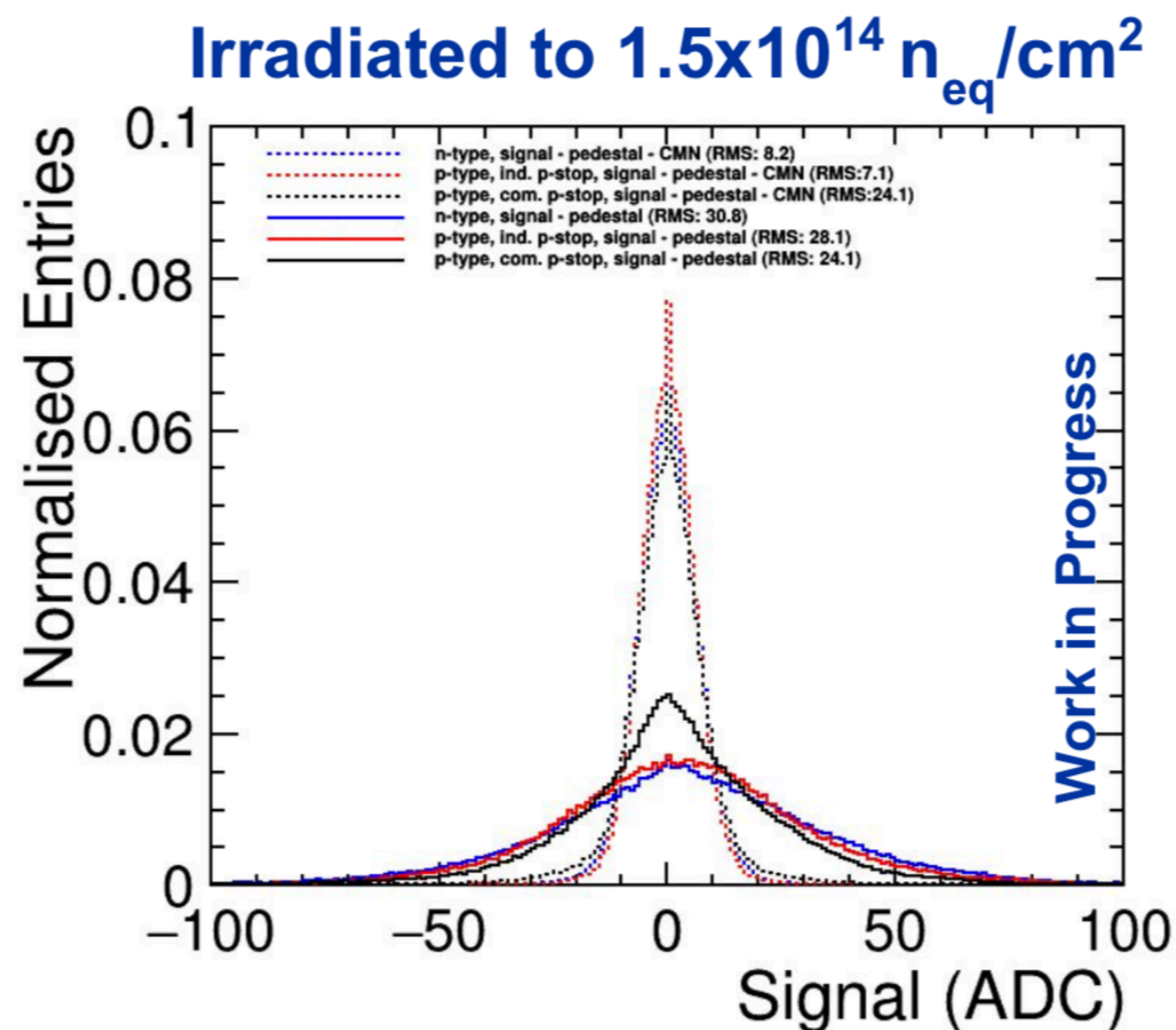
Hexaboard Probe Card



Noise of Unirradiated Sensors @ 400V

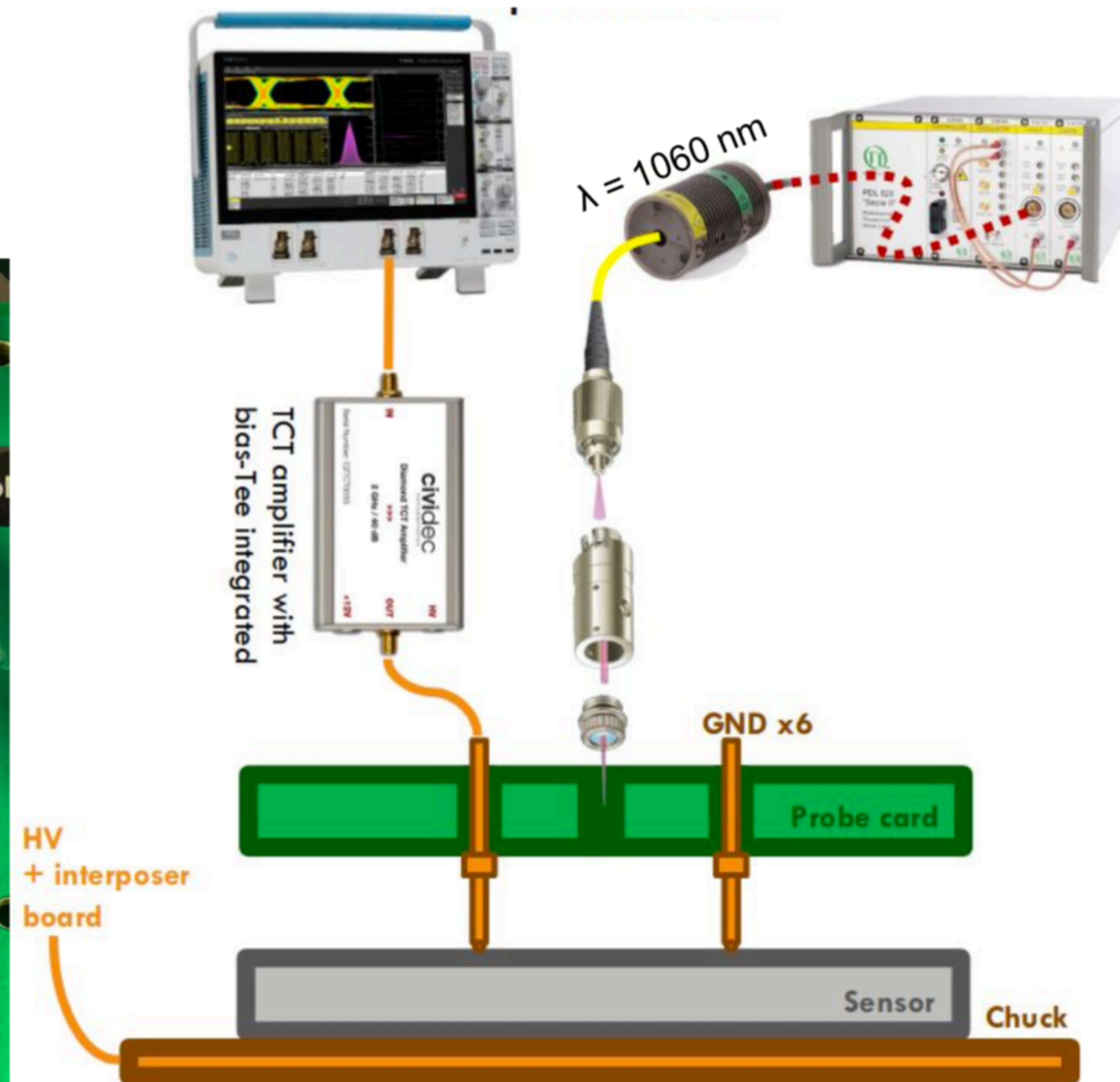
- **1 MIP in 300 µm sensor corresponds to ~40 ADC**
- **So far no significant difference between p-type and n-type was observed**
  - Studies done in CMS Tracker group showed that non-Gaussian noise caused by micro-discharges due to high electric field is larger in n-type sensors
- **Next: sensors irradiated to higher fluences**





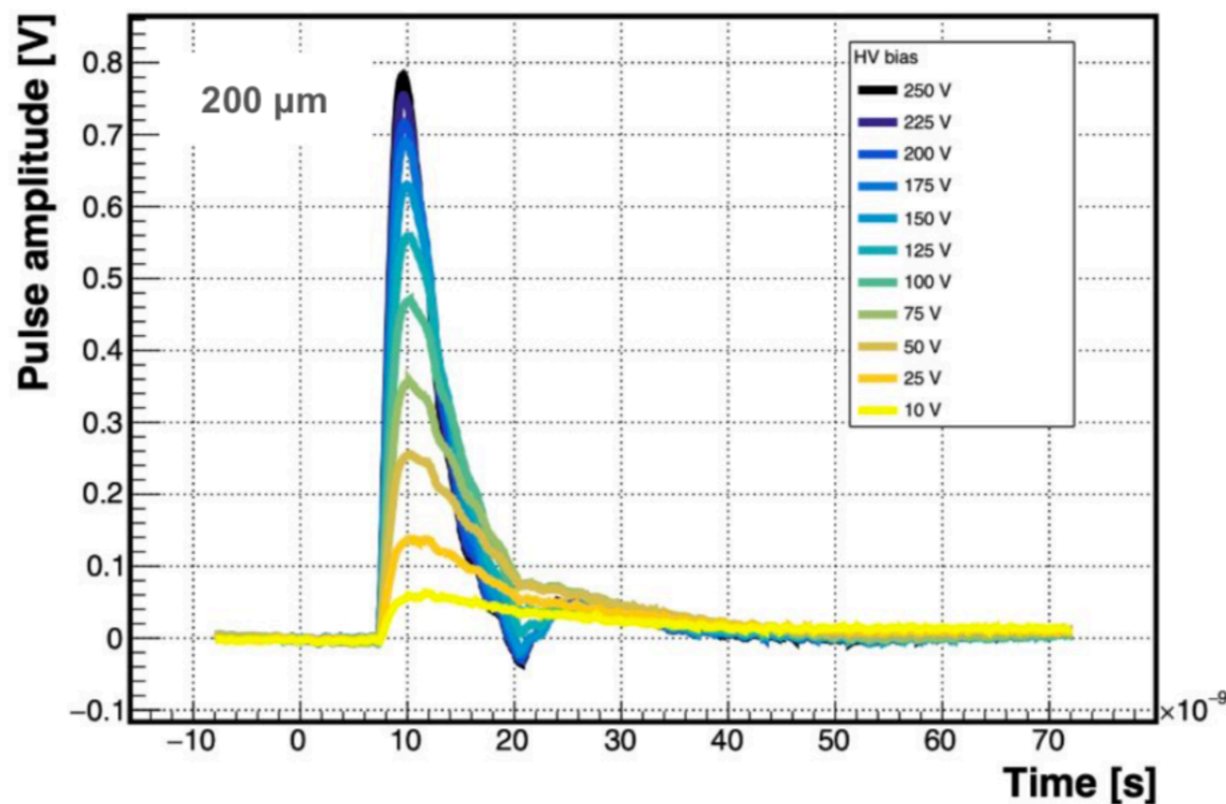
Transiant Current Technique, 7-pin board

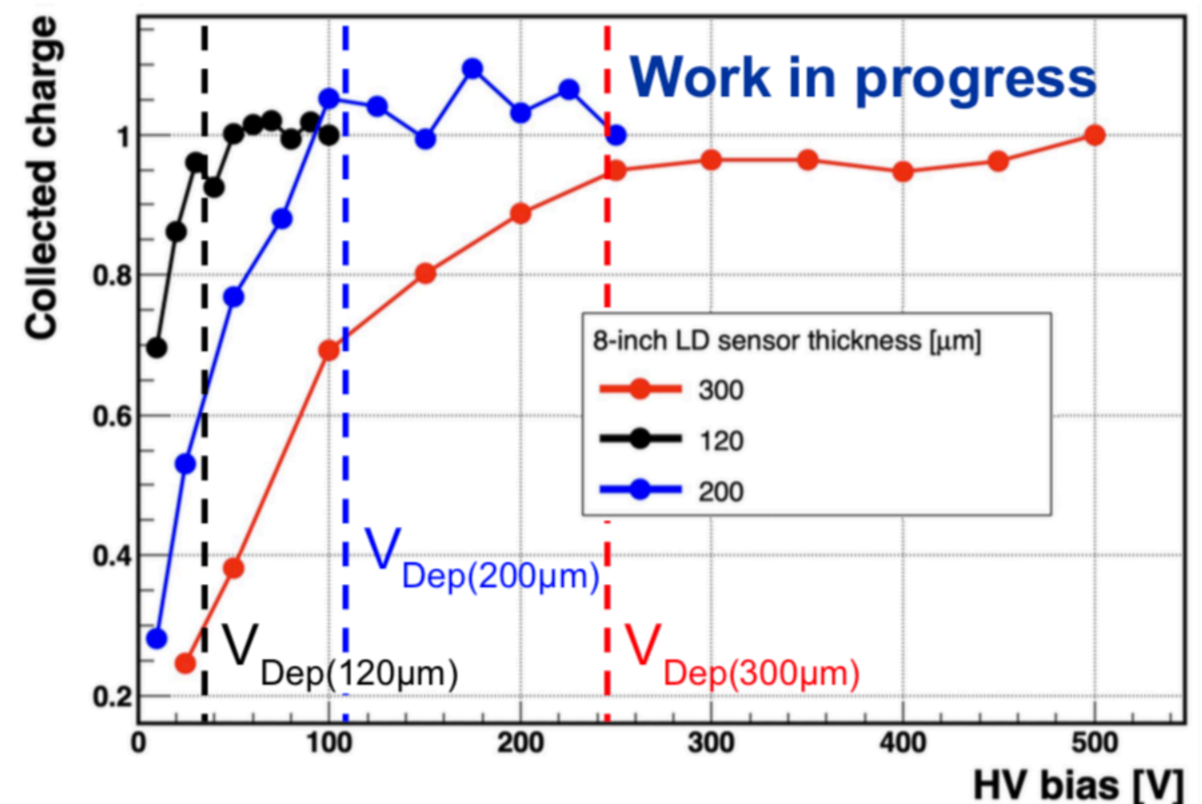
- **TCT: a signal is generated in the silicon sensor with a laser and the induced current is recorded by an oscilloscope**
  - Can study charge collection efficiency
  - Probe different sensor depth with different wavelengths
- **7-pin TCT board**
  - Developed at Fermilab
  - Adoptable to different sensor layouts



CCE Measurements on 8” Sensors

- **Collected charge increases with depleted volume**
- **Voltage scan reveals depletion voltage (saturation of collected charge)**
- **Collected charge calculated from full waveform integral (normalized to value at highest HV)**





Summary

- The HL-LHC poses high pile-up and high radiation level challenges
- The HGCal design is well prepared to cope with the challenges using high granularity, precision timing and silicon sensors
- Versatile systems developed for characterization of large area silicon sensors
- Fast turnaround for CMS HGCAL sensor production phases
- Next steps: further characterization of irradiated sensors