The SBND Hardware Trigger

CPAD 2019

David Rivera on behalf of the SBND collaboration

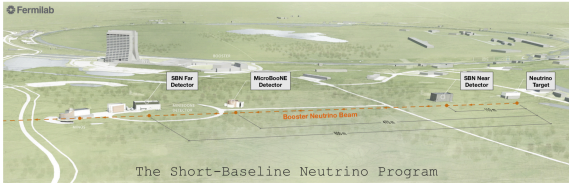
University of Pennsylvania

December 9, 2019

Table of Contents

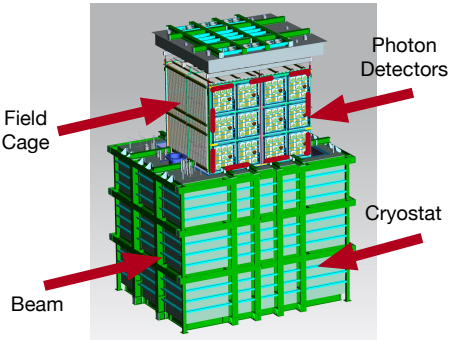
Short Baseline Neutrino (SBN) Program

- Three surface detectors: SBND, MicroBooNE, and ICARUS
- Liquid Argon Time Projection Chambers (LArTPC) in the Booster Neutrino Baseline (BNB) at Fermilab
- **Goal:** unambiguous discovery of **sterile neutrinos** or a 5σ exclusion of the 3+1 oscillation parameter space allowed by the LSND and MiniBoone anomalies



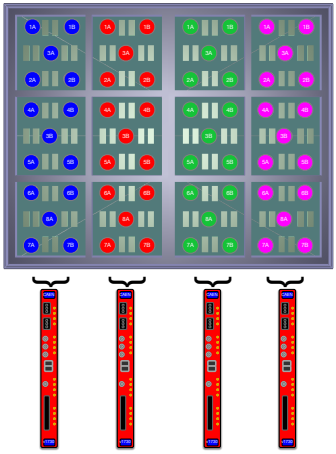
Short Baseline Near Detector (SBND)

- SBND will sample the unoscillated flux of neutrinos 110m from the target
- 112 tons of active LAr divided into two, 2m drift regions
- 11,264 channels of charge readout
- Complementary Cosmic Ray Tagger (**CRT**)
- Complementary Photon Detection System (**PDS**) - 120 PMTs + 192 ARAPUCAS



SBND - exploded view

PDS Readout



Example mapping of PMTs to CAENs

- PMT waveforms are digitized by commercial CAEN V1730 modules
- 16 ch/board
- Each CAEN V1730 provides:
  - PMT pair majority trigger (at least N pairs have crossed threshold)
  - Analog output proportional to number of self-triggered pairs

Cosmic Ray Tagger

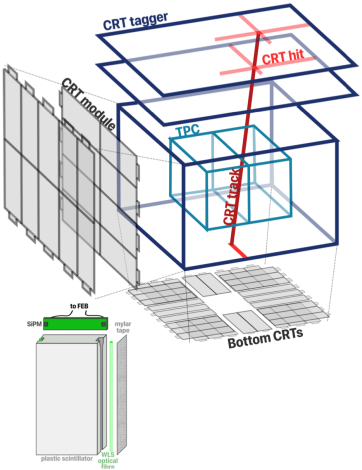


Photo credit: Tom Brooks

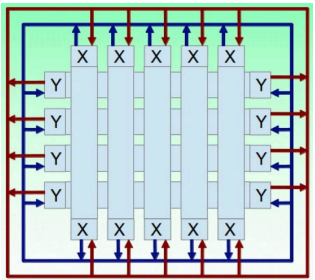


Photo credit: Igor Kreslo

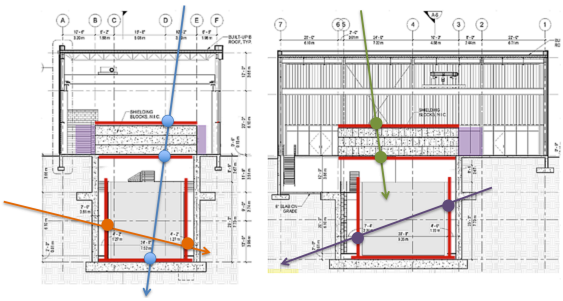
- Roughly 90% coverage
- CRT hits are recorded when there is a coincidence in ANY X and ANY Y for a given panel

CRT Triggering

Suggested triggers by Michelle Stancari.

Calibrating with the CRT

- Through-going muons parallel to the wire plane are useful for determining electron lifetime
- Cathode-crossing muons are useful for alignment in time and space



- CRT-A: Vertical through-going
- CRT-B: Stopping muons (Michel sample)
- CRT-C: Horiz. through-going Anode-Cathode crossing muons
- CRT-D: Horiz. through-going “parallel” muons

Requirements

- 1.596 μs/spill$\cdot 1.32 \times 10^8$ spills = 211 seconds "in-spill" over the three years
- Neutrino interactions/spill = 7,251,948/1.32×10^8 = 0.055
  - $\sim$ 1 neutrino interaction every 18 spills
- Our data diskwrite budget is roughly 5Hz and will include:
  - Beam neutrino candidates
  - Random Triggers
  - Calibration Triggers (see slide 7)
- PDS and CRT requirement: $\sim$1ns timing resolution

The Penn/Photon Trigger Board

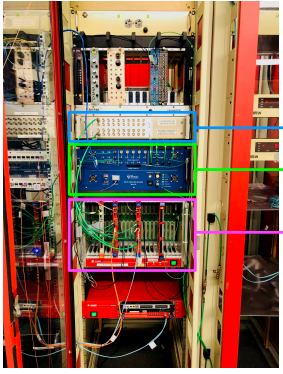
Some design considerations:

- Can make a prompt trigger decision based on Auxiliary detector information
- Something flexible, configurable, and compact
- Easy to interface with the DAQ
- Documents the trigger decision and what led to it

The PDS Trigger Hardware

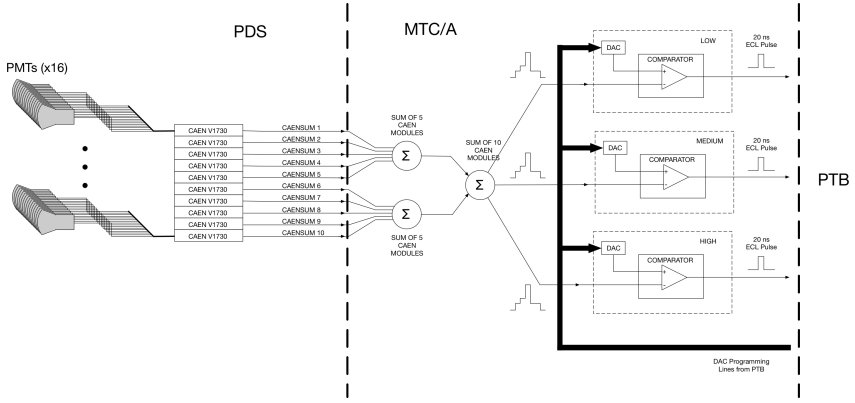
Analog Master Trigger Cards (MTC/A)

The Penn/Photon Trigger Board (PTB)



PDS Vertical Slice Rack

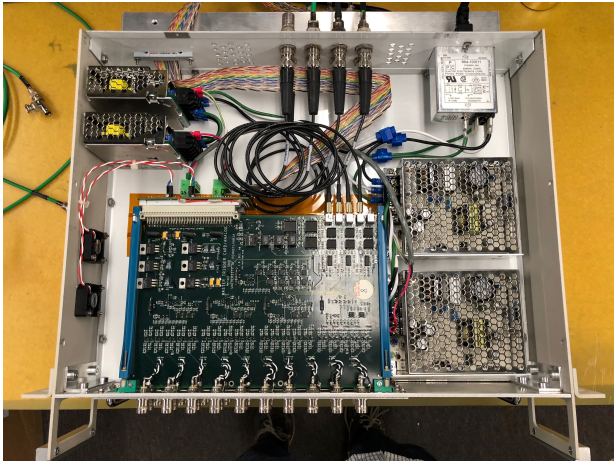
MTC/A Summing



- Perform fast analog sums of the number of PMT pairs that have crossed thresholds across multiple V1730s
- Fully asynchronous, cascaded commmon base pair summing

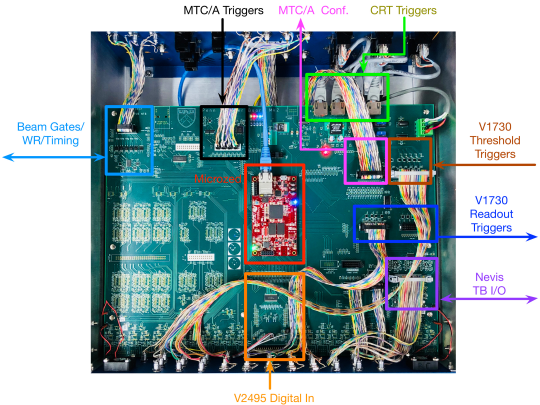
Analog Master Trigger Cards (MTC/As)

- 20 input channels per MTC/A
- Three DC thresholds (LO, MED, HI) per MTC/A that represent three numbers of PMT pairs
- Useful for identifying events that produce localized flashes
- Useful for events that trigger many PMT pairs across multiple boards

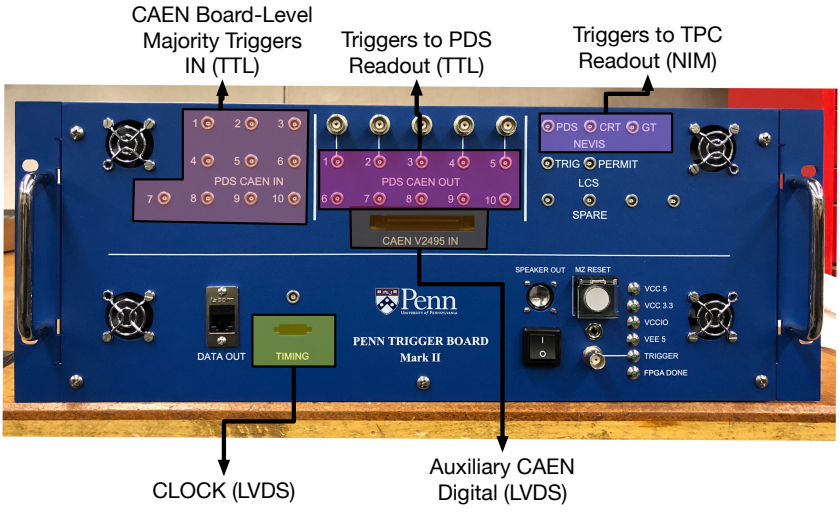


Penn Trigger Board IO

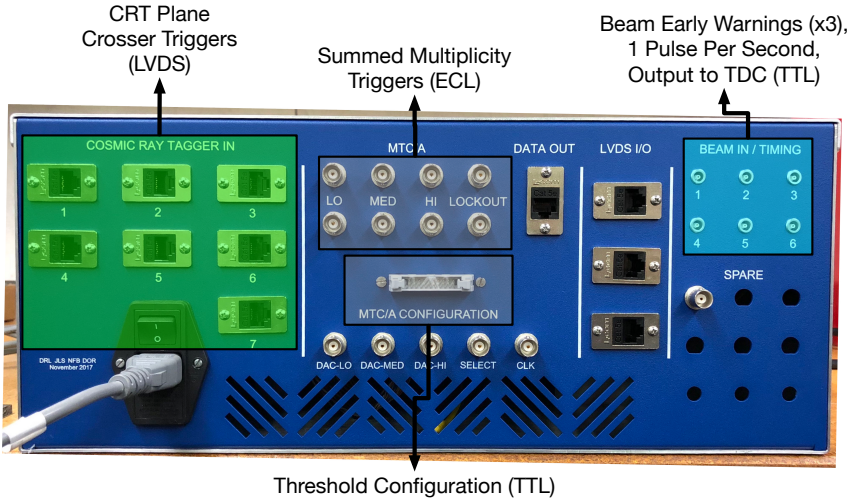
- 33 Input Trigger Primitives:
  - 10 PDS Threshold Triggers
  - 6 MTC/A PMT Multiplicity triggers
  - 14 CRT Triggers (X & Y for each of 7 Planes)
  - 3 Accelerator Complex Early Warnings
  - (Possible Upgrade) 32 additional inputs from CAEN V2495
- 1 Pulse Per Second (1PPS) and reference clock from the timing system



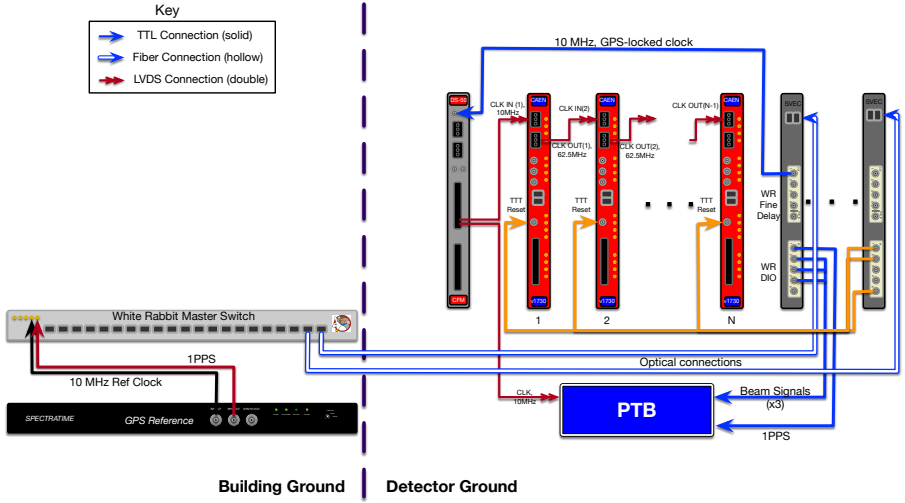
Penn Trigger Board IO (Continued)



Penn Trigger Board IO (Continued)



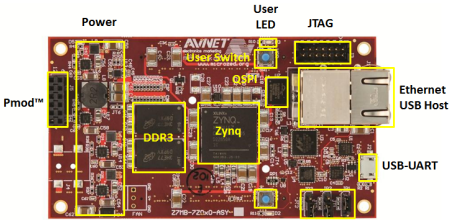
Synchronization Scheme

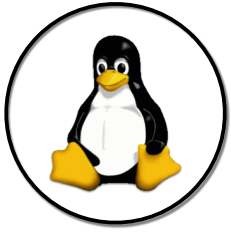


- The timing system will distribute reference signals (e.g. 1PPS)

PTB Core

- Microzed onboard the PTB contains SoC (System-on-Chip)
  - Processing System (PS) - boots a Linux kernel and root filesystem
  - Programmable Logic (PL) - FPGA with high-bandwidth/high-performance interconnects to PS
- FPGA firmware can be flashed remotely
- Data Acquisition runs as a process initialized on power up
  - Soft Reset, Initialize, Start Run, and Stop Run
- Communicates through a TCP socket with a client running on the DAQ server





PTB Overview

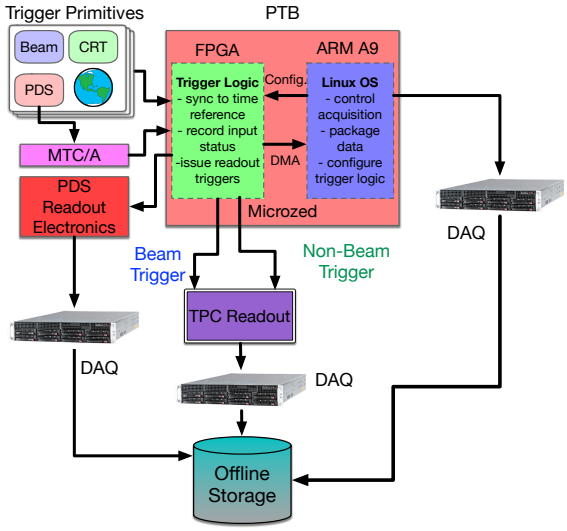


Table of Contents

Input processing

- All inputs are latched on a 50MHz clock
- Masks – decide which input channels participate
- Input Delay Compensation – delay signals by N clock cycles
- Signal Shaping – defines coincidence gates (stretch to pulse N clock cycles long)

All are input configuration parameters passed to PTB by the DAQ through a **.JSON** file

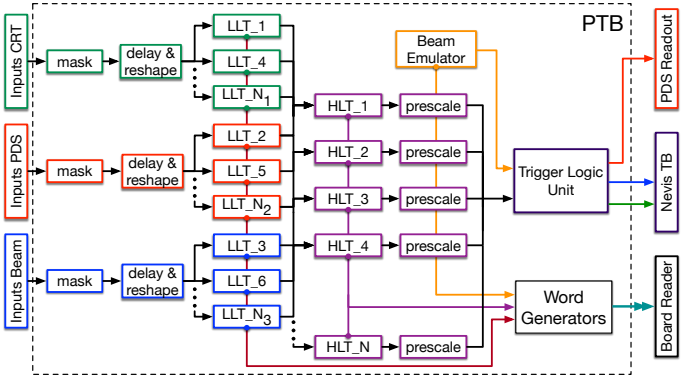
Triggers

Low Level Triggers (LLTs):

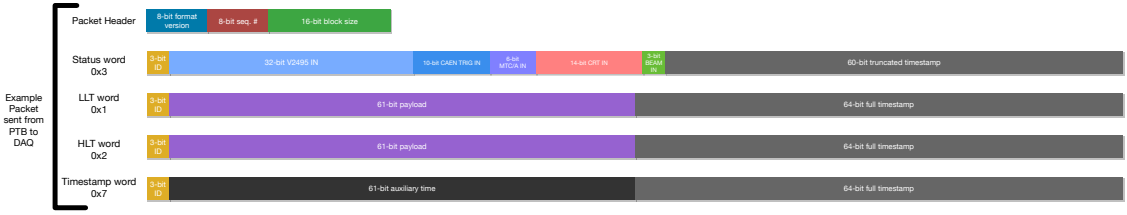
- Single subsystem

High Level Triggers (HLTs):

- Drive the readout decision of the TPC and the complementary subsystems
- Based on LLTs and can be across multiple subsystems
- Can be prescaled

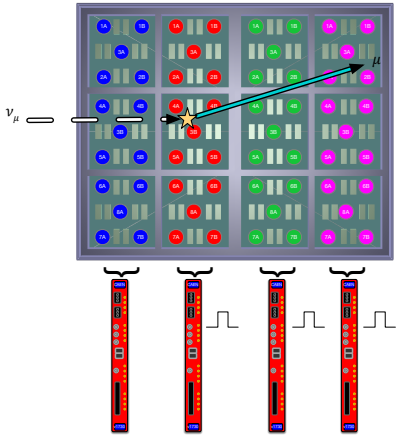


Trigger Words



- Low Level Trigger (LLT) Words
- High Level Trigger (HLT) Words
- Timestamp Words – sent periodically to keep data moving
- Channel Status Words:
  - **debug** mode any time there is a transition in any of the inputs from low to high,
  - **standard** mode – in ProtoDUNE status words are issued only when an HLT is generated

PDS Triggering Example

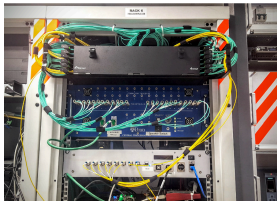


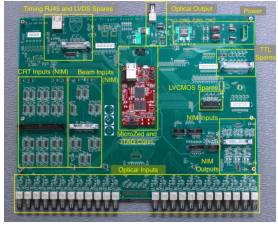
Neutrino interaction

- Requiring excess light in coincidence within the 1.6μ spill:
- $\geq$ 3 CAENs on the beam side meet majority mode

Testing

- Scatter Gather DMA allows us to read out at much higher rates (>1MHz of 128-bit words)
- Triggering logic is all synchronous - 100ns of latency
- The Central Trigger Board in ProtoDUNE is the same PCB and has been running successfully in ProtoDUNE-SP





Central Trigger Board for ProtoDUNE-SP

Table of Contents

SBND Integration Tests

We have a DAQ test stand to commission each hardware readout component (TPC, PDS, and CRT) as well as the trigger

Plans going forward

- The trigger is currently being incorporated into our event simulation

A complementary software filter is under consideration

- To achieve full granularity on the CRT at the strip level
- To achieve higher granularity on the PDS at the PMT level

Summary

- The PTB is flexible and fast
- The hierarchical trigger successfully ran succesfully in ProtoDUNE
- The PTB will:
- improve event selection in SBND
- Drive the prompt readout of all photodetectors

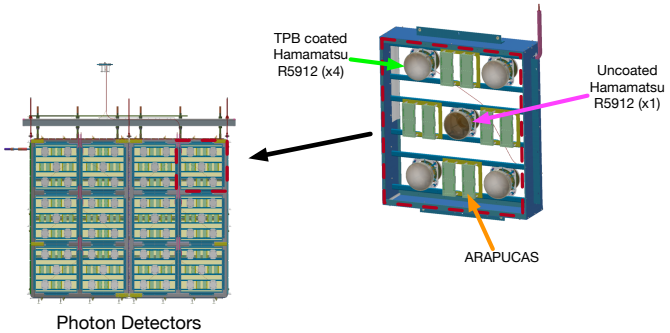
Table of Contents

Backup

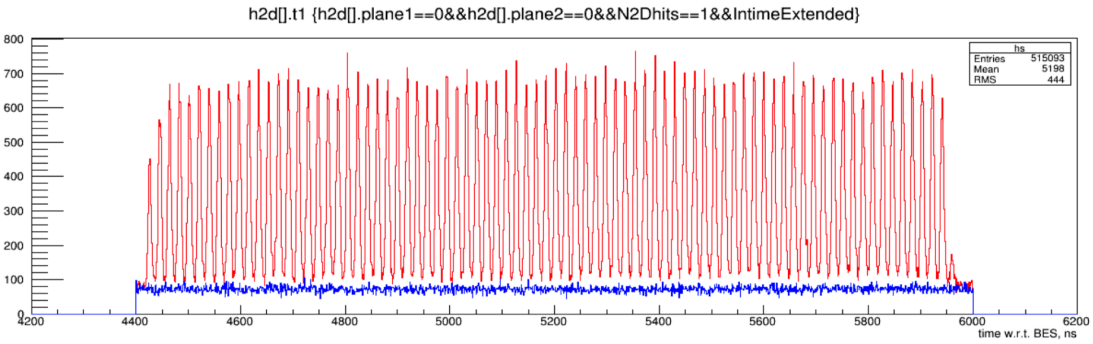
Photon Detection System in SBND

Rich photon detector system with:

- 120 Photo Multiplier Tubes (PMTs) – (96 TPB-coated + 24 uncoated)
- 196 ARAPUCAS – light traps with dichroic filter (3 variants)

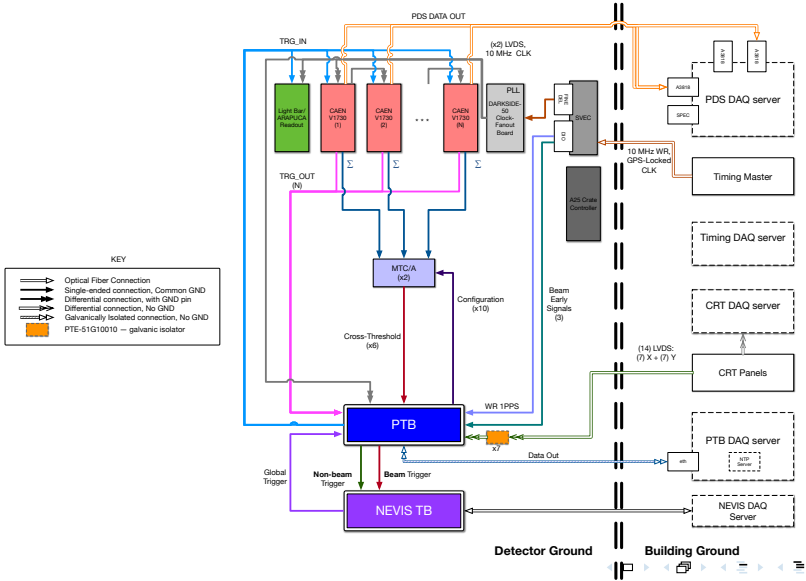


Event selection



- PDS and CRT can give us a t_0 for cosmics entering the detector
- Can discriminate cosmic ray activity with t0 outside of bunch width
  - caveat : need good spatial resolution as well
- **Online:** can choose to veto events crossing a certain level of activity from the CRT

Trigger System Overview

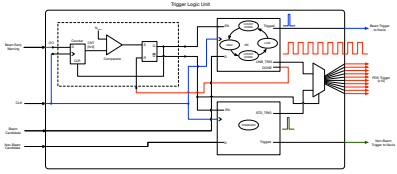


Timing Scheme

- For PDS Trigger system, WR will be used to distribute the 1PPS and the 10 MHz, GPS-locked clock
- A fanout module can be used to sync all 8 CAEN digitizers + PTB
- If the 1PPS and the GPS clock stay edge-aligned, we can use the GPS clock to interpolate
- PTB's internal timestamp clock will be phase-locked to GPS clock and will run at 50 MHz
- WR 1PPS signal will simultaneously:
  1. Reset 28-bit rollover (fine time) counter
  2. Query NTP time on Linux Side

Trigger Logic Unit (TLU)

- Configure whether PDS trigger is required or not for trigger pulse-train to CAENs
  - Utilize originallly allocated ports PDS→Beam, CRT→Non-beam
  - Similar to what is done in ProtoDUNE; CTB issues beam or non-beam commands to timing system
  - Mitigates need for veto logic to be implemented in external NIM hardware



Functional diagram of PTB trigger logic unit state machine.

What can we trigger on?

- Beam Early Warning signals – simplest beam trigger
- We expect scintillation light from our neutrino interactions
  - Trigger on coincidences between PDS and spill arrival (derived from Early Warning signal)
- Coincidences in X and Y panels of the CRT
- CAEN board-level majority triggers
- MTC/A multiplicity sum over pairs of PMTs
- Random (or fixed-frequency) triggers (in- or out-of-spill)
- Nevis Global Trigger
- Spare NIM inputs
- CAEN V2495 (possible upgrade) – can perform additional digital logic across multiple CAEN V1730

Maximum CAEN Throughput: 80 MB/s
Maximum Trigger Bandwidth per board:

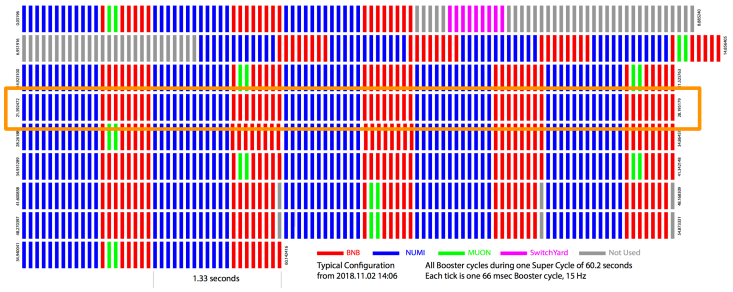
$$\begin{aligned} r_{\text{board}} =& 1\text{board} \times 16\frac{\text{ch}}{\text{board}} \times 16\frac{\text{bits}}{\text{sample} \cdot \text{ch}} \times 500\frac{\text{samples}}{\mu s} \times \frac{1}{\text{board} \cdot \text{trigger}} \\ =& 1.28 \times 10^5 \frac{\text{bits}}{\text{trigger} \cdot \mu s} \times \frac{1\text{B}}{8192\ \text{bits}} = 15.625\frac{\text{kB}/\mu s}{\text{trigger}} \end{aligned} \tag{1}$$

Solving for the maximum number of triggers per board per second **per μs being read out**:

$$\begin{aligned} 80\ \text{MB/s} =& r_{\text{board}} \times \text{N}_{\text{triggers}} \cdot \Delta t \\ \Rightarrow& \frac{\text{N}_{\text{triggers}}}{\text{sec}} \cdot \frac{\Delta t}{\mu s} = 5242.88 \end{aligned} \tag{2}$$

BNB/NuMI Structure

- BNB/NuMI beam extraction examples in figure 11 below
- 1.33s cycles divided into 20, equally-spaced spills



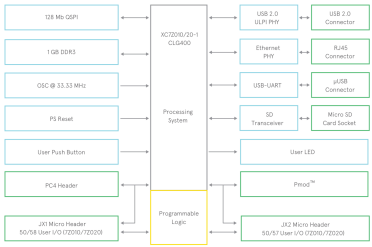
Bill Badgett's graphical represenation of BNB/NuMI cycles

- 8/20 spills extracted per 1.33s cycle 6Hz (best case)
- Expect more like 5Hz

Microzed Details

- Processing System (PS) - onchip BOOT ROM + dual core ARM Cortex A9 processor + 256KB SRAM used to run a Linux distribution
  - Xilinx First Stage Boot Loader intializes the PS and flashes the PL firmware
  - U-Boot takes over in the second stage to read and load the kernel image and the root file system
- We utilize Ubuntu 16.04 as our Linux distribution

BLOCK DIAGRAM



Booster Neutrino Beam

- Protons are accelerated up to 8GeV (KE) in the Booster ring and extracted for the Booster Neutrino Beamline
- 8GeV protons strike the Be target at MI-12
- Charged pions are focused and serve as our (anti)neutrino source upon decaying in flight

Parameter	Value
Exposure	6.6×10^{20} P.O.T
Spills	1.32×10^{8} spills
Avg. Spill rate	5Hz
Spill duration	1.596μs
Bunches/spill	84
Bunch spacing	19ns
Bunch spread	1ns

Neutrino Interactions

Estimated Neutrino Events for SBND with 6.6×10^{20} P.O.T. delivered over 1.32×10^{8} spills.

Process	No. Events	Events/spill	Stat. Uncert.
ν_μ CC Inclusive	5,212,690	3.95×10^{-2}	0.04%
ν_μ NC Inclusive	1,988,110	1.51×10^{-2}	0.07%
ν_e CC Inclusive	36,798	2.79×10^{-4}	0.52%
ν_e NC Inclusive	14,351	1.09×10^{-4}	0.83%
Total	**7,251,949**	$\mathbf{5.5}\times10^{-2}$	**0.03%**

- Numbers taken from table of the SBND Conceptual Design Report (here)

Back of the envelope trigger rate

- Assumptions:
  - 100% trigger efficiency on all ν events
  - 10kHz of cosmics entering the active volume (AV)
  - Full readout = three, 1.28 ms readout windows per global trigger

- 211 seconds of "in-spill time"
- 7,251,948 interactions $\times 3 \times 1.28\text{ms} = 27,848s$ of readout
- No. cosmics $\sim 10\text{kHz} \times 27,848s = 2.78 \times 10^8$ cosmics
- Avg. spill rate $\times$ No. neutrino interactions / spill $= 5\text{Hz} \times 0.055 = 0.275\text{Hz}$

- ~38 cosmics piling up in our full readout window along with our neutrino event!
- What can we do about it?

Timing Scheme Continued

- Possible to account for latency between the PTB and the WR nodes by echoing back to WR and measuring this externally with sub-ns precision (e.g. a Time-to-Digital Converter)

$$T_{\text{global}} = (\text{Counts since last PPS}) \times \text{clock period} + T_{NTP} + \text{Offset} \tag{3}$$

Where: T_{NTP} = Global time rounded to the nearest *proper* second, and *Offset* accounts for latency for receiving 1PPS signals **Note:** The NTP server will have ~(10 ms) accuracy, PTB will talk to this server through Linux side

PTB Firmware