Chronopixel CMOS Sensor Development for the ILC

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EE work has been contracted to Sarnoff Corporation/SRI

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Note: Many of these slides are based on originals prepared by Nikolai Sinev and Christian Weber
International Linear Collider

First stage - 250 GeV (Higgs Factory)
Ultimately higher energy: 0.5 - 1 TeV

ILC250

Damping Ring

e- Source

e+ Main Linac

e+ Source

e- Main Linac

~20km

SiD at ILC
“Model-independent” EFT fit

~1% required to access New Physics beyond HL-LHC direct search


arXiv:1903.01629
Processes and Approximate Timelines Toward Realization of ILC (Physicists’ view)

Government Level

Announcement by Japanese government

- Discussion among governments
  - Exchange of information
- Strengthen US-Japan Discussion Group, cost reduction R&D, governance discussion
- Establish Discussion Group with the European partners

MoU among research labs on start of the preparation phase under approval by each government

European Particle Physics Strategy Update

- SCJ Master Plan
- LCB/ICFA mtgs. @ Tokyo

- Draft proposal by researchers on international cost sharing
- Talks with other countries

Physicists Level

Start negotiations among governments on international sharing

Agreement on governance, operation, sharing of cost and human resources

-full-scale negotiation among governments – specification of conditions and processes

Critical decision process

European Particle Physics Strategy Update

- EPPSU submitted to CERN

- ILC pre-lab (4 years)

- SCJ committee on ILC
- MEXT panel

Start construction of ILC

Final agreement among governments on construction

Good enough design for the final approval of construction, resolution of remaining technical issues

* ICFA: international organization of researchers consisting of directors of world’s major accelerator labs and representatives of researchers
* ILC pre-lab: International research organization for the preparation of ILC based on agreements among world’s major accelerator labs such as KEK, CERN, FNAL, DESY etc.
Status of ILC decision in Japan

- Legislative branch (Diet) strongly supports hosting ILC in Japan.
- Two final national steps are needed to reach decision.
- (1) Science Council of Japan (SCJ) calls for proposals of large-scale research projects every three years, and recommends “priority programs” to MEXT. In the latest process in 2017, 20 programs were selected from 200 proposals.
- ILC will be evaluated for first time this year to provide evidence of support by broader Japanese academics.
- SCJ selected ILC for the reduced long list after 1/3 selection and invited ILC for an “interview.”
- Results of final SCJ evaluation will be publicized officially in February 2020.
- (2) Next step will be MEXT Roadmap in 2020. Previous 2017 Master Plan/Roadmap process, MEXT made its own selection starting from the SCJ long list to create MEXT Roadmap.
ILC Beam environment:

Bunch crossing rate (Collisions rate) \(\sim 3\ \text{MHz}\)
Number of bunches in bunch train up to \(\sim 3000\)
(first 250 GeV stage 1312)
Bunch trains interval – 200 ms. (5 Hertz)

Detector System

5 layers, \(\sim 2.4\ \text{cm} - \sim 10\ \text{cm}.\)
Length: \(\sim 20\ \text{cm}\) with forward discs.
Pixel size \(< 15 \times 15\ \mu m^2\) (space point resolution \(\sim 3.5\mu\)).
Each pixel has 2x12 bit memory buffer to record 2 time stamps during bunch train.
Room temperature operation with forced air cooling and non-turbulent air flow.
Power dissipation for entire Vertex Detector to \(< \sim 100\ \text{W}.\)
Sparse readout allows full readout in 200 ms.
S/N ratio should be more than 30 (noise less than 25 e\(^{-}\)).
Chronopixel development history

2004 – First discussion with Sarnoff Corporation. Oregon University, Yale University and Sarnoff Corporation collaboration formed.

2007-2010 - Prototype 1
5x5 mm chips, 80 each, containing 80x80 50 µm Chronopixels array

TSMC 0.18 µm ⇒ ~50 µm pixel
Epi-layer only 7 µm
Low resistivity silicon (~10 ohm-cm)

2010-2013 - Prototype 2
MOSIS / TSMC. (48x48 array of 25 µm pixel, 90 nm process)

2014- Prototype 3
Summary of prototypes 1 and 2 tests

Prototype 1 demonstrated:

- Time stamp recording with 300 ns period (1 ILC bunch crossing interval)
- System to read all hit pixels during 200 ms interval between bunch trains (by implementing sparse readout)
- Pulsed power (2 ms ON and ~200 ms OFF) with preserved comparator performance.
- Noise figure achieved as 24 electrons rms, compared to spec of 25.
- Comparator offset spread a few times larger than anticipated.

Prototype 2 demonstrated:

- All NMOS electronics without unacceptable power consumption
  - (not clear all NMOS electronics is a good alternative to deep P-well option)
- Comparators offset calibration with virtually any required precision using analog calibration circuit.
- Smaller feature size creates issues: sensor capacitance limits signal/noise ratio, stemming from 90 nm process design rules.
Six different sensor options were implemented on the same chip – 8 columns for each option:

1. Same as prototype 2 – for comparison.

2. Deep NWELL diode in the window in P++ layer - design rules waiver.

3. Shallow NWELL diode, also in the window - design rules waiver.

4. “Natural transistor” in the P++ layer window transistor is formed directly on P+ epi layer large source and drain diffusion areas gate connected to both source and drain and form sensor output.

5. Also “Natural transistor” but with 2 fingers source and drain are narrow gate also connected to both, as in option 4.

6. Same as 5, however gate is not connected to source and drain, but connected to external bias voltage.
Deep NWELL (option 2) larger area and larger charge collection efficiency, but larger capacitance.

Shallow NWELL (option 3) smaller area, but P++ acts as charge reflector. Window size may define charge collection efficiency.
Options with “Natural transistor”

Option 4 (1 finger)
Larger nwells forming source and drain. Is charge collection efficiency better? What is impact of size on sensor capacitance?

Option 5 (2 finger, gate to source and gain)

Option 6 (2 finger, gate to external bias)
How do these two options behave?
Fe55 sensor capacitance test

\[ C = \frac{E_{\text{Fe55}} \cdot 1.6 \cdot 10^{-19} \cdot C}{3.6 \, eV} \]

\[ E_{\text{Fe55}} = 5.9 \, keV \]

<table>
<thead>
<tr>
<th>diode option</th>
<th>Capacitance (fF)</th>
<th>μV/e</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9.0</td>
<td>18</td>
</tr>
<tr>
<td>2</td>
<td>6.2</td>
<td>26</td>
</tr>
<tr>
<td>3</td>
<td>2.7</td>
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<tr>
<td>5</td>
<td>4.9</td>
<td>33</td>
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<tr>
<td>6</td>
<td>8.9</td>
<td>18</td>
</tr>
</tbody>
</table>
Sensor noise measurements

Noise larger, than expected from kTC noise formula. Additional noise pick up.

<table>
<thead>
<tr>
<th>Option #</th>
<th>Noise r.m.s (mV)</th>
<th>Noise r.m.s (# electrons)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.12</td>
<td>63</td>
</tr>
<tr>
<td>2</td>
<td>1.08</td>
<td>42</td>
</tr>
<tr>
<td>3</td>
<td>1.7</td>
<td>29</td>
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<tr>
<td>4</td>
<td>1.21</td>
<td>37</td>
</tr>
<tr>
<td>5</td>
<td>1.23</td>
<td>38</td>
</tr>
<tr>
<td>6</td>
<td>0.98</td>
<td>54</td>
</tr>
</tbody>
</table>

Option 3
min Cap

Option 6
max Cap
## Noise observed vs expected

<table>
<thead>
<tr>
<th>Option</th>
<th>sigma obs. (mV)</th>
<th>sigma exp. (mV)</th>
<th>Sqrt ((\delta^2_{ob} - \delta^2_{ex})) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.12</td>
<td>0.67</td>
<td>0.9</td>
</tr>
<tr>
<td>2</td>
<td>1.08</td>
<td>0.8</td>
<td>0.73</td>
</tr>
<tr>
<td>3</td>
<td>1.7</td>
<td>1.21</td>
<td>1.2</td>
</tr>
<tr>
<td>4</td>
<td>1.21</td>
<td>0.9</td>
<td>0.8</td>
</tr>
<tr>
<td>5</td>
<td>1.23</td>
<td>0.9</td>
<td>0.84</td>
</tr>
<tr>
<td>6</td>
<td>0.98</td>
<td>0.67</td>
<td>0.72</td>
</tr>
</tbody>
</table>

### Anomalous extra noise, near pulse control

### Max extra noise, min cap

**Extra noise pick up appears to occur mainly through capacitive coupling to the sensor**
Best performance from option 3
   shallow NWELL,
   small capacitance, large signal,
   violates design rules

However, option 3 sensor area is only 2.74 µm²,
while options 4 and 5 – natural transistors – have sensor (n+ diffusion
area) 19.36 µm², important for charge collection.

Also, p++ implant reflects charge - competes with sensor size.

Future studies needed to investigate the relevance of the competing
features to produce optimal design.
Neutron Irradiation Test

- 4 MeV proton incident on $^7$Li target to produce neutrons
- Proton beam current and neutron rate monitored during irradiation test
- Total number of neutrons created is eventually determined by radiation assay of target
- Chronopixel works after $10^{13}$ $n_{eq}$/cm$^2$


Lithium target

Figure 4. A calculated neutron energy histogram.
Test resistance w.r.t. total ionizing dose received

1 MeV protons
4 nA current
(large dose rate!)

Energy deposited within first 8 μm of silicon
(≈ epi layer)

After each irradiation run

Anneal at 60°C for 80 min
Test for change in count rate using Sr-90 source
\( t_{1/2} = 29 \text{ yrs}, 2.3 \text{ MeV } \beta, \text{ minimum ionizing} \)
MeV proton irradiation results

- sensor type 1
- sensor type 2
- sensor type 3
- sensor type 4
- sensor type 5
- sensor type 6

ATLAS phase 2 pixel detector, outer layer
ATLAS phase 1 pixel detector, inner layer
# ILC Chronopixel performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ILC Requirement</th>
<th>Prototype Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detector Sensitivity</td>
<td>10 μV/electron</td>
<td>59 μV/electron</td>
</tr>
<tr>
<td>Detector Noise</td>
<td>25 electrons</td>
<td>29 electrons</td>
</tr>
<tr>
<td>Comparator Accuracy</td>
<td>0.2 mV RMS</td>
<td>0.2 mV RMS</td>
</tr>
<tr>
<td>Sensor Capacitance</td>
<td>10 fF</td>
<td>2.7 fF</td>
</tr>
<tr>
<td>Clocking Speed</td>
<td>3.3 MHz</td>
<td>7.3 MHz</td>
</tr>
<tr>
<td>Charge collection time</td>
<td>300 nsec</td>
<td>20 nsec</td>
</tr>
<tr>
<td>Readout Rate</td>
<td>25 Mbits/sec</td>
<td>25 Mbits/sec</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.13 mW/mm²</td>
<td>OK by estimate</td>
</tr>
<tr>
<td>Radiation Hardness</td>
<td>$10^{11}$ neutrons/cm²/yr</td>
<td>$10^{13}$ neutrons/cm² or 110 Mrad</td>
</tr>
</tbody>
</table>
Conclusions

Following a multi-year R&D effort, Chronopixel prototype 3 demonstrated a working ILC CMOS vertex sensor that satisfies the ILC design requirements.

Radiation exposures have shown the performance is maintained for ILC exposure levels.

Future development will further improve and refine the details:

- Refine analysis of option trade-offs.
- Thicken epi layer and increase resistivity.
- Expand detector area.
- Reduce small cross talk issues.
- Perform tests with minimum ionizing particles.
- Demonstrate min-ion efficiencies.

We gratefully acknowledge support by the Department of Energy, Office of High Energy Physics.