Towards Pixel Triggering

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Important Factors

- Possible Use Cases for Pixel Triggering (in typical collider detector geometry, pixels nearest IR)
  - Improved Impact Parameter Resolution
  - Separated Vertex Tagging
    - b/c/tau jet taggers
  - Improved Primary Vertex Reconstruction
  - Improved Vertex Separation for pileup mitigation in multi-object triggers
    - Requires matching pixel tracks to other L1 objects
  - Electron/Photon Discrimination
    - Electrons have pixel hits; photons do not

- Physics needs should drive development paths
  - Expensive in material, power, and complexity for pixel systems that are already very challenging to construct (more on this presently)

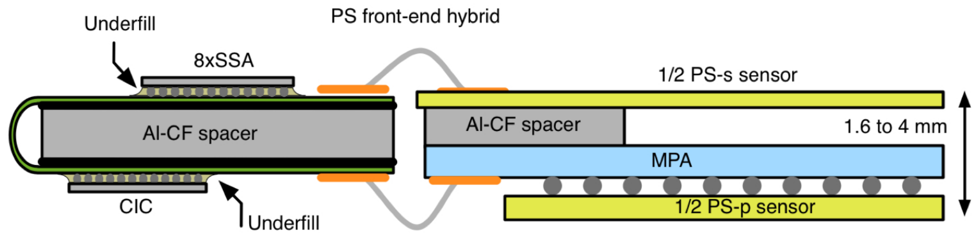
Challenges

- The challenge
  - Making pixel systems triggerable at L1 for future experiments at future machines
- Requires more readout bandwidth
- Why this is difficult
  - Very compact systems, close to the interaction region
    - High radiation environment (HL-LHC: 1 GRad, 2E16 n/cm^2)
    - High flux of particles (HL-LHC: 2E9 hits cm^{-2}s^{-1})
    - High data rates
  - System-level and integration issues
    - Higher bandwidth readout → higher power
    - Local processing → higher power
    - Higher power → more cooling & cables / converters
    - Added on-detector functions require more inactive material → system optimization must include impacts of "services"

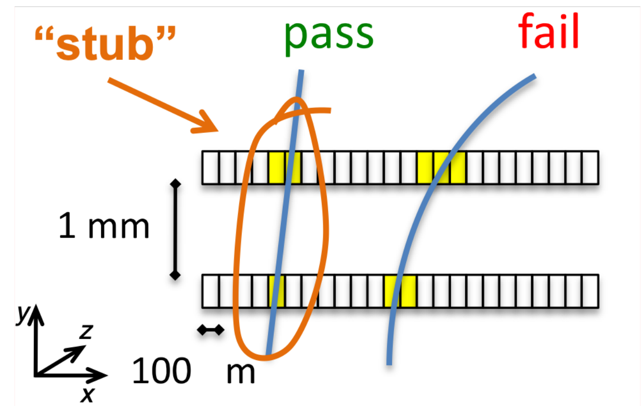
Bandwidth Requirements

- Present LHC systems trigger at ~100 kHz
  - CMS: 1.8m^2, 123×10^6 pixels, 1200*400 Mbps links
  - Already using on-ASIC zero suppression
- HL-LHC Systems Trigger at ~1 MHz
  - CMS: 5m^2, 2×10^9 pixels, ~1400*10 Gbps links
  - Bandwidth driven by
    - Higher flux/instantaneous Luminosity (2E34 → 5E34 cm^{2}s^{-1})
    - Higher trigger rate (0.1 → 1 MHz)
    - More tracking stations (4 layer/12 disk) from larger η coverage
- Consider a System providing info to L1 at 40 MHz
  - Simplistic scaling: 40x more bandwidth needed
  - Reducible in principle with
    - Reduced information sent for L1 decision (macro pixels)
    - On detector processing: e.g. clusterization, layer correlators
    - Region of Interest readout architectures e.g. L0 trigger to RoI
  - Likely need several factors to reach overall goal of 40

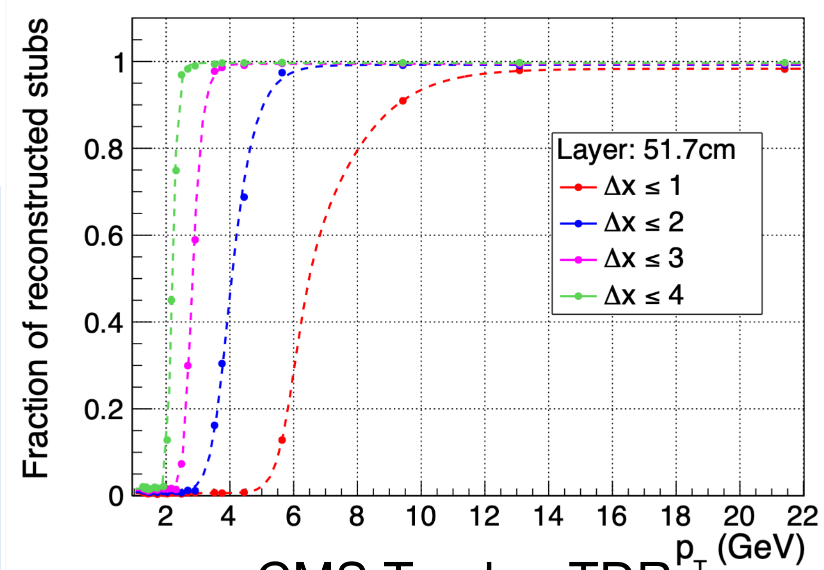
Local Processing



- Example of Track Triggering
  CMS HL-LHC Outer Tracker
  - Already makes use of pixels
    - CMS PS modules have pixels & strips
    - Used in 3 inner layers
  - Local processing in p_T doublet modules
  - CMS Design filters on p_T and transmits tracklet stubs to L1 track finder
  - Large data reduction from sending all stubs
    - Still 90% of BW is used to transmit L1 stubs from modules to track finder
    - For this design ~10x more BW needed to implement a triggering tracking detector



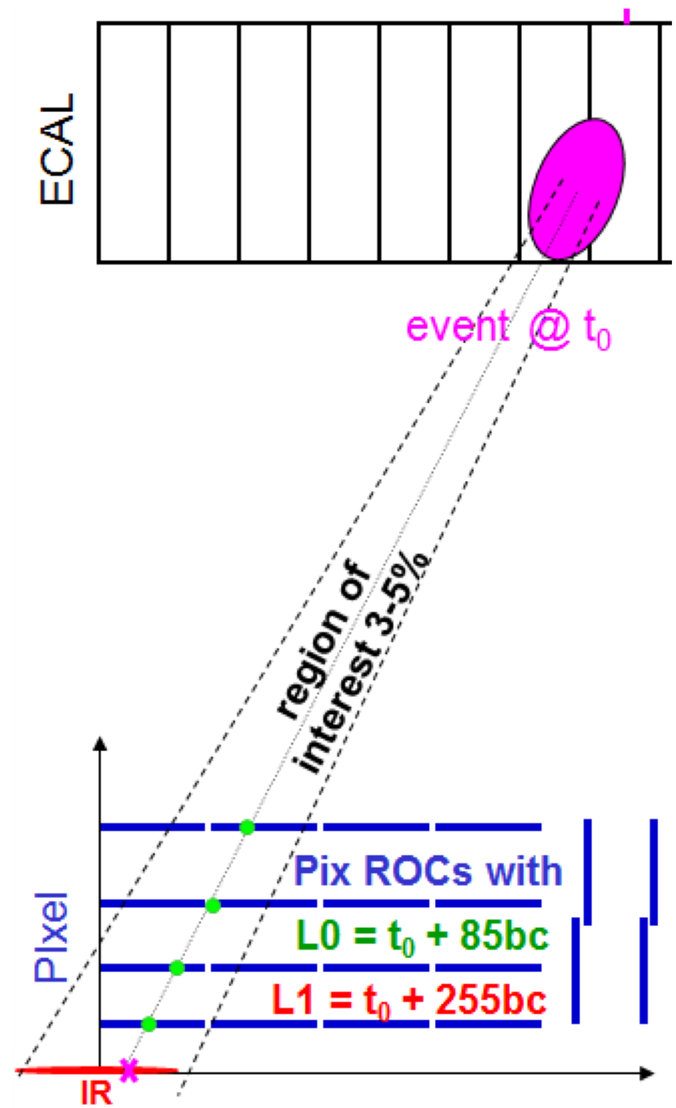
- Similar factors maybe possible in future pixel trackers
  - Challenges to corollate among layers
    - Doublet modules?
    - Inter-layer links in sectors – optical, electrical?
  - Forming pixel clusters in ASIC may reduce data to send & ease use in L1 trigger



CMS Tracker TDR

Region of Interest Readout

- Reduce bandwidth by sending trigger info after L0 trigger in limited regions of interest
  - L0 issued by other trigger systems (+latency)
  - Sector based tracking readout for area pointing to L0 objects, e.g. γ/ electron candidate, jet, …
- Natural granularity in modular pixel systems E.g. HL-LHC CMS IT
  - Φ ~ 12 facets
  - η ~ 20 for |η|< 4 N.B. *not* uniform
  - One (η, Φ) region ~ 0.5% of detector
- Defining RoI by (η, Φ) sectors has non-trivial implications for detector layout
  - Better: project L0 objects back onto modules
  - Send L0 by module ID (e.g. via LUTs)
- Advantage disappears if too many objects need pixel info for L1 decision – just read it all out
- RoI definition is a system level design decision



R. Horisberger / W. Smith c. 2010

R&D Areas

System level issues discussed earlier
Additionally some generic R&D on links & ASICs that would enable future triggering pixel systems

- Local Processing
- RoI Architectures
- Radiation-hard high-speed low-power links
  - Many HL-LHC systems rely on the 10 Gbps lpGBT and Versatile Link+ projects
    - Low power gigabit transceiver ASIC 65 nm 1.2 V
    - VL+ Laser diodes adapted from COTS 2.5V with 65 nm ASICs supporting (transimpedance amps & laser drivers)
    - Lasers to 100 MRad & 1E15 had/cm^2 → HL-LHC lasers not on pixel modules
  - Next generation links for particle physics are needed
    - Higher bandwidth
    - Low power
    - Higher radiation qualification
- Next-generation ASICs for HEP
  - Enable local processing for data reduction
  - More logic density from smaller feature size (RD53 is 65nm)
    - Must qualify transistors for TID and SEU/SET effects
    - Triple Modular Redundancy provides SEU mitigation with more gates

Summary

- The use case(s) for pixel triggering should be carefully considered and motivate system design
  - A pixel tracker system optimized only for track reconstruction performance is not the same as an *triggering* pixel tracker system optimized for physics performance including triggering!
- Pixel systems are squeezed for space, power, cooling, readout bandwidth
- Radiation tolerance of optical links and ASICs are key enabling technologies
- System-level design can be guided from the current (next) generation of tracking detectors
  - Here I refer to the design process not just “scaling it up”
  - Local processing was a keystone for making track trigger readout feasible for CMS HL-LHC OT
  - RoI L0 readout may be an idea worth exploring (again)
  - Other innovations should be explored