Trigger Hardware GCT Muon and Future Developments

System Design and Status

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Primary Design Goals

- Modular
  - Reasonably fine grained
    - Smaller circuit boards
    - Easier and less expensive to develop
  - Should scale well
- Well defined internal interfaces
  - Allows modules to be developed independently
    - Perhaps shared across projects
  - At least electrically compatible
- Flexible in both logic and interconnect
  - Retain flexibility of FPGAs
  - Add complementary data routing flexibility
    - Modify data flow without altering hardware
    - Give the ability of dynamic reconfiguration

Relevant Current Technology

- Large FPGAs with built in SERDES links
  - Very high density logic
  - SERDES I/O allows physical concentration of data
    - 16-24 3+Gbps links available on large devices
    - Normal I/O pins support 1+Gbps links
- LVDS/CML crosspoint switches
  - Up to 144x144 non blocking matrices
  - Asynchronous, Protocol agnostic
    - Multi rate switching supported intrinsically
  - Currently available at 4+Gbps, 10Gbps announced
- Fractional-N frequency references
  - Wide range (10 – 700+MHz)
  - Meets Xilinx serial link reference specifications
  - Allows interoperability with many standards

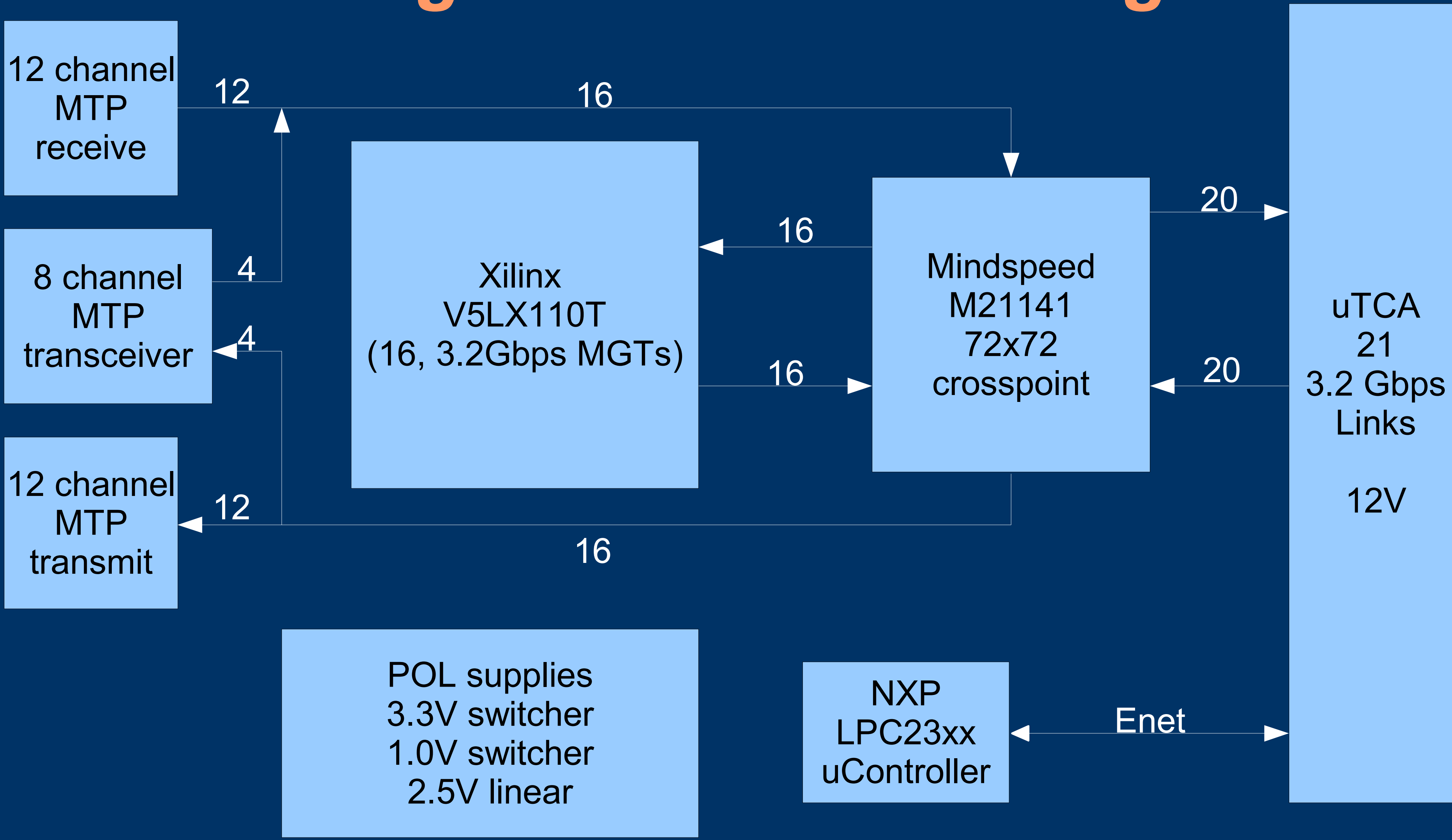
Implementation

- Micro TCA based, 12 slot chassis
  - 20 high speed links per slot
- Processing module
  - Based on Xilinx V5LX110T
  - Mindspeed M21141 72x72 crosspoint
  - MTP Fiber interface (SNAP-12)
  - Local precision serial link reference
- Backplane
  - Commercial unit possible, but limiting
    - Can host Processing modules
  - Custom unit based on Mindspeed M21161 144x144
    - Programmable topology
    - 500 Gbps maximum bandwidth
    - Includes simple uTCA hub functionality
    - External and internal reference oscillators

uTCA Infrastructure etc

- Sequenced power up
  - Intelligent power management by backplane/hub
    - Sense circuitry detects module insertion
  - Microcontroller powered up first
    - Known as "management power"
  - Main power supplied after software handshake
    - Our backplane will initially implement dumb power
    - Eventually will need more formal attention
- Slow control interface
  - Based on Ethernet protocols
  - Implemented in NXP 2368 by software
    - Prototype TCP/IP sockets and Telnet interfaces running
    - Eventually will need more formal attention

Processing module Block diagram



Key Features of Processing Module

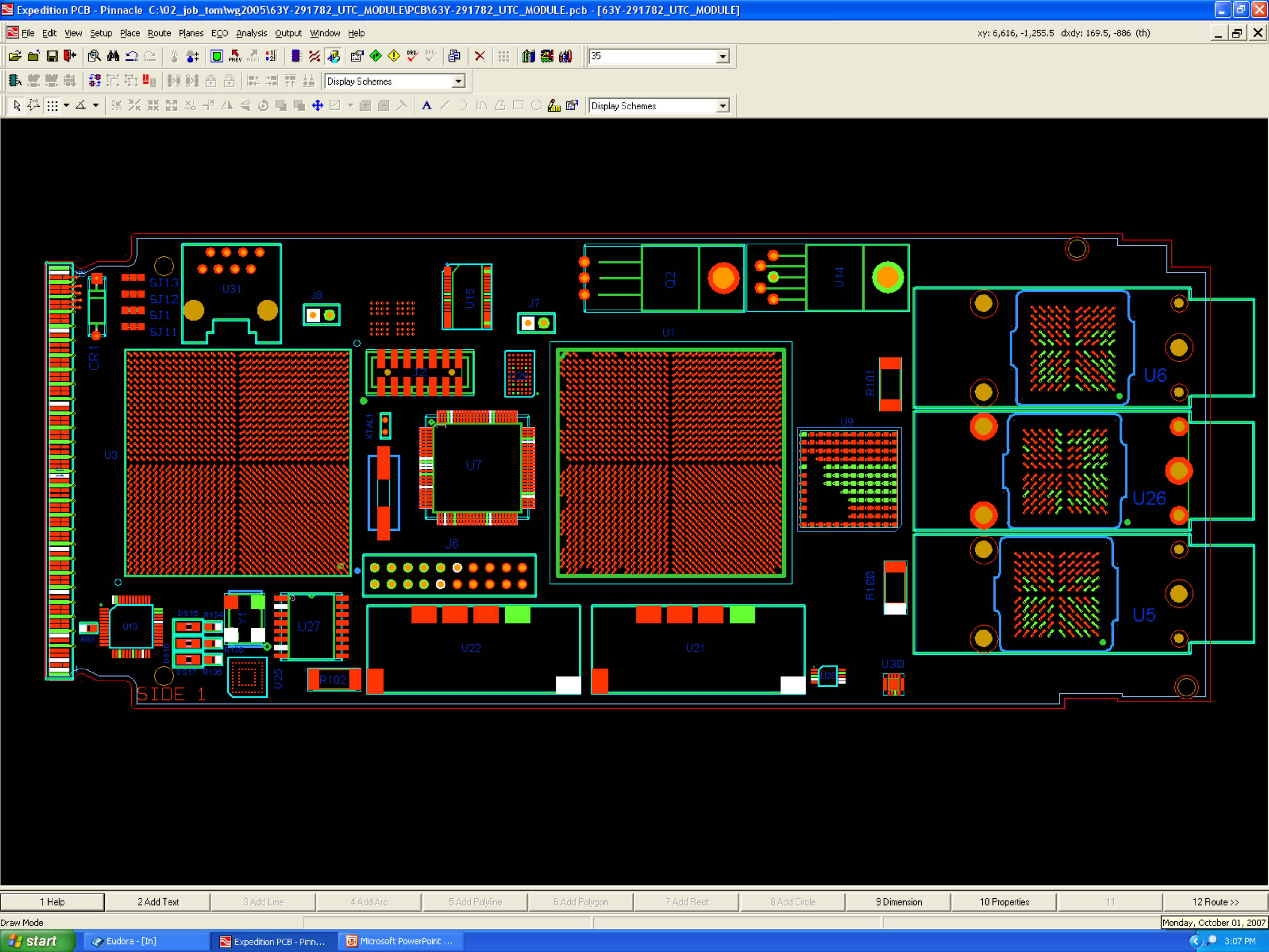
- Xilinx Virtex 5LX110T FPGA
  - 16 low power MGTs, Superior logic density/speed
  - Standard I/O 1Gbps capable
- Data I/O direct from fiber
  - 16 channels full duplex @ 3.2 Gbps
- Crosspoint routes to FPGA, backplane, and fiber
  - 1:N data replication supported at wire speed
  - FPGA output data sent to backplane or fiber
  - Switches clocks as well as data
    - Dedicated low jitter clock tree provided for MGT reference
    - Clock output to backplane from crosspoint
- Slow control via standard Ethernet
  - Standard Ethernet protocols supported by NXP 2368
  - Connection provided for stand alone operation

Additional Features

- These features are unused in the Muon System
  - Future use, no development for GCT
- Module development is co-funded by Los Alamos
  - Intended for signal processing research
  - Independent funding for this application
- Additional RAM
  - 512MB DDR2 SDRAM added to module
    - Two banks of 128Mx16 @ >500MHz
    - Enables sophisticated SoC possibilities
  - ~100 high speed (500 MHz), length matched traces
- Initially unused Xilinx V5 features
  - PCIExpress endpoint
  - GigE MAC

Advanced PCB Techniques

- Los Alamos has evaluated 2 new Techniques
  - Standard process for current fabrication technology
  - Less demanding than multi laminate process used on leaf
- Micro Vias
  - Penetrate several layers (2-3)
    - Provide lowest inductance/best impedance match
    - Useful for both power and high speed signals
  - Laser drilled
- Via in pad
  - Micro via or drill via
  - Eliminates BGA escape pattern for higher performance
- Both technologies are being used in the design
  - Vendor (DDI) considers this the lowest risk approach


Expedition PCB - Pinnacle C:\02_job_tom\wg2005\63Y-291782_UTC_MODULE\PCB\63Y-291782_UTC_MODULE.pcb - [63Y-291782_UTC_MODULE]
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Display Schemes
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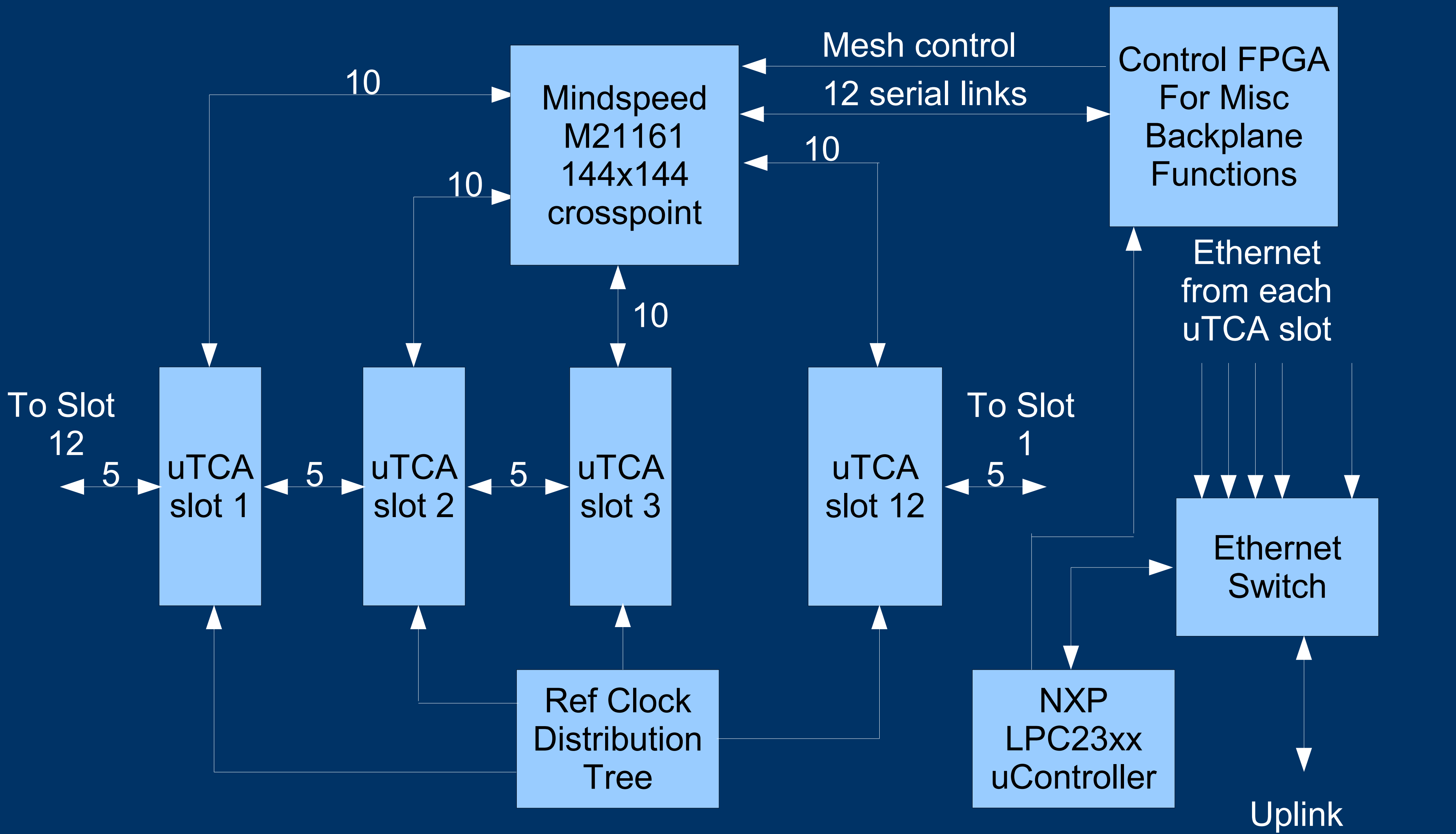
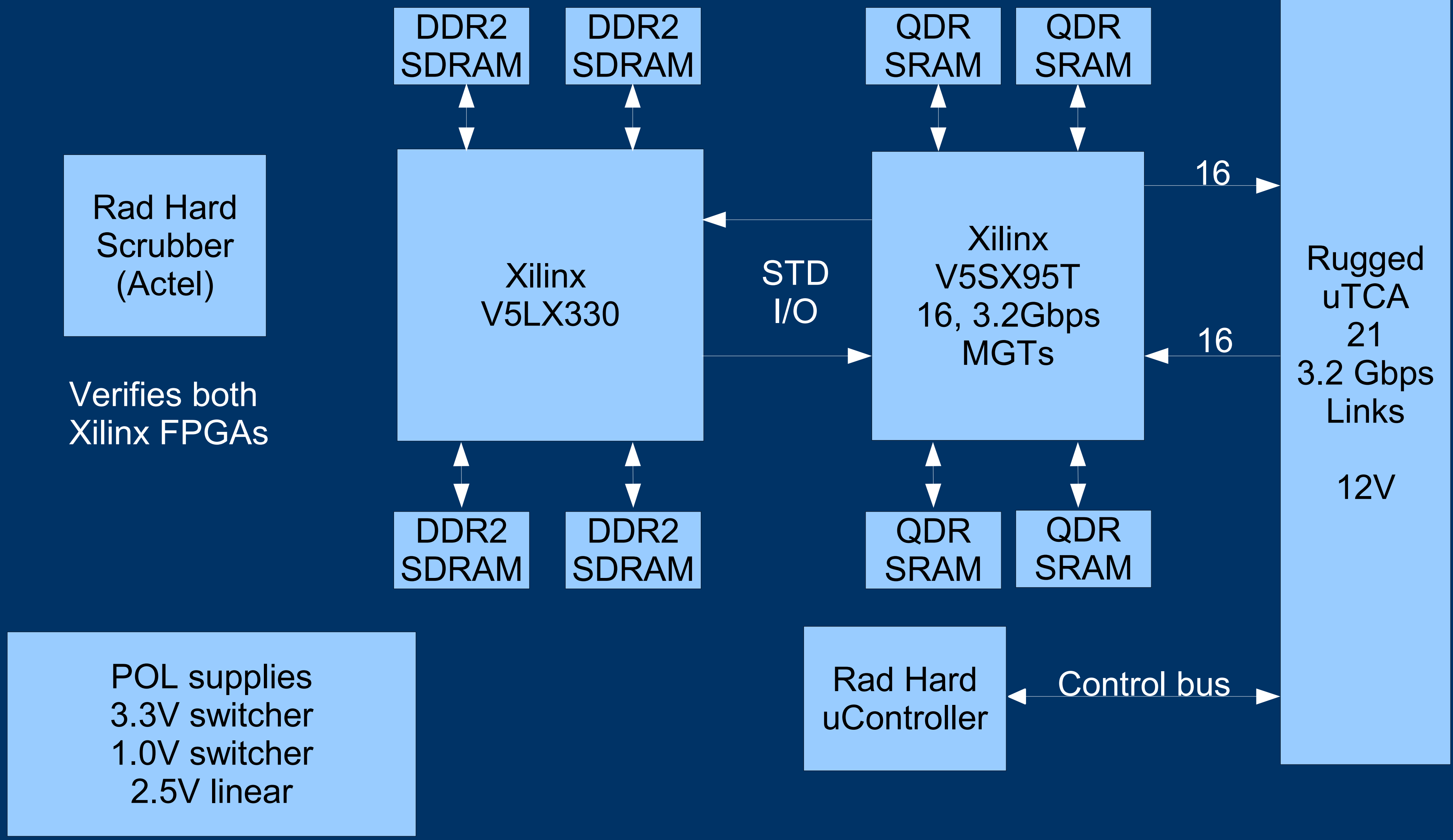
Custom Backplane block diagram



Key Features of Custom Backplane

- Active backplane based on crosspoint switches
  - Mindspeed M21161 (4.1 Gbps)
  - Active backplane eliminates congestion
- Simple clock tree
  - Micrel Sy87739 Fractional-N synthesizer
    - 10-700+MHz range for flexible system operation
  - External input
  - 1 clock/slot driven by crosspoint
    - Suitable for general purpose clocking
- Double height, ½ crate width
  - Link routing easier
  - Use inserts to accommodate single high modules
  - Better overall density per crate
- 20 links/slot for high speed data communication

Additional Development - LANL SDR Processing Module



System Design Challenge

- Many Large FPGAs pose several challenges
  - Firmware development
    - Large, complex designs
    - Modular components desirable
      - Implies more disciplined collaboration
    - Distribution and Configuration control non trivial
  - System state of health
    - Verify all FPGAs loaded with proper firmware
    - Check to insure configuration is intact
      - Cross section will be considerable
      - SEUs will occur
- Numerous high speed links
  - Robust operation required
    - Avoid using links in electrically non-standard modes
    - Consider tagging data to facilitate automatic recovery

FPGA Design Techniques

- Use software system development as a model
  - Create a repository for shared modules
    - Hosted at a common point (could even be Google?)
    - Open source, accessible to all
  - As in software, this could consume much manpower
    - Need to establish and enforce reasonable goals
- Should include self verification in all designs
  - Xilinx V2 and above have internal config interface
    - Part can read it's own config memory
    - Checksum verification possible
  - Several levels of checking are possible
    - Based on granularity of check
  - Parts are not 100% checkable
    - 90% confidence achievable
      - Can't check distributed or block RAM
    - This is improving with latest silicon

Link Management – GCT Lessons

- Link PLL reference critical
  - Variable (VCXO) references should be avoided
    - Links perform coarse calibration at initialization
      - Drift eats directly into link frequency margin
    - Require reinitialization to recover from excessive drift
      - This is a non-specified parameter on most hardware
  - GCT runs links at 100MHz fixed frequency
    - ~80MHz data rate
    - Firmware inserts “idle”commas when required
- Avoid hard synchronization to timing system
  - Compound errors occur during timing “hiccups”
    - Lost link sync and data synchronization
    - Complicates fault characterization and recovery
  - Links need to be transparent data pipes
    - Design to manufacturers specs for maximum reliability

Link Management – Data Format

- Following GCT lessons provides an opportunity
  - Implement to the extent possible
- Run links as fast as possible on fixed reference
  - Reduces intrinsic latency
  - Use extra bandwidth for robust features
    - CRC
    - Sequence number or time tag
    - Data type, source, etc.
- Variable topology complicates synchronization
  - Sequence information embedded in data a benefit
    - Allows realignment
    - Can enable firmware compensation for dropped packets
- Advanced techniques possible
  - Zero suppression and data compression
    - Currently being considered for Los Alamos work